Matrix Converter Based Open-end Winding Drives

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Dedication

To my family.

Abstract

A significant portion of all electric power generated is consumed by electric motors employed in commercial, industrial, and transportation sectors. Variable frequency drives (VFDs) are desirable, and in many cases necessary, for superior control performance and efficiency. At present, most VFDs use a 'line frequency AC' → 'DC-link' → 'variable frequency AC' architecture, where the front-end converter may or may not support bidirectional power flow and input power factor control. In these drives, the load-end converter is almost always a two- or multi-level voltage source inverter (VSI). The front-end converter may be another VSI, or a line-commutated rectifier. This is a robust architecture that has benefited from extensive use; consequently, the inverter design and control methods are quite standard, and the behavior of all components in the drive system is generally understood.

VSI based drives need large capacitors to support the DC-link voltage and significant reactance at the drive input to limit the harmonic current drawn from the grid. The switching common-mode output voltage generated by these drives causes bearing currents and ultimately motor failure. Therefore, even though the drive topology is quite robust, the system suffers from downtime and high maintenance costs because of the unreliable capacitors and bearing failure; and large volume because of the large capacitor and line reactor requirement.

Matrix converters offer 'line frequency AC' → 'variable frequency AC' conversion without an intermediate DC-link, although an actual or implied soft link may exist. These converters use reactive components only for filtering the harmonics of the PWM frequency. Furthermore, when modulated using rotating vectors, the output common-mode voltage is ideally equal to zero. A major limitation of this modulation technique is a poor voltage transfer ratio of 0.50, and therefore modulation using stationary vectors has received more attention, even though the latter generates switching common-mode voltage at the output, and allows input power factor control only at the expense of the voltage transfer ratio.

The output common-mode voltage can be eliminated while maintaining a good voltage transfer ratio using a direct matrix converter based open-end winding drive reported

in 2010. This drive topology is also capable of input power factor control; and is expected to have significantly lower reactive element requirements compared to VSI based drives.

Indirect topologies for matrix converter based open-end winding drives are also possible. These topologies utilize a three-level inverter structure and employ three converters: the front-end converter converts the input voltages to ordered three-level link voltages. The two load-end converters convert the link voltages to variable frequency voltages to be applied at the two sets of motor terminals. The additional advantages of the indirect approach are a more mature structure, clamp circuit elimination, robust and efficient commutation, lower voltage stress on the switches, and lower losses. The indirect topologies also lend themselves to low-voltage-ride-through without any additional switches.

This dissertation presents experimental results from two distinct indirect matrix converter based open-end winding drives. The results demonstrate good common-mode performance, high voltage transfer ratio, and input power factor control.

Having established the feasibility of the indirect approach for matrix converter based open-end winding drives, the two indirect drives reported here and the direct drive reported in literature are compared on semiconductor requirements, semiconductor losses, and input/output harmonic content. The most promising matrix converter based open-end winding drive is then compared with state-of-the-art systems on the same criteria, as well as on passive elements, control, and instrumentation requirements.

To this end, a new filter design procedure with optimal damping for matrix converter applications is also developed in this dissertation. A comparison of the reactive components used by this filter to the reactive components used in back-to-back VSI systems shows that the matrix converters' passive element requirements are in fact lower than the back-to-back VSI based systems.

In summary, this dissertation demonstrates the feasibility of two distinct drive topologies with significant advantages using experimental results. The practical questions pertinent to any new design are answered, and the conclusions have been used to identify the best matrix converter based open-end winding drive topology. Qualitative and quantitative comparison with the state-of-the-art systems reveal a clear advantage in the common-mode voltage related effects and the passive components' sizing.

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Chapter 1

Introduction

This chapter describes the state-of-the-art AC/DC/AC drive systems and discusses their drawbacks. Direct AC/AC drive systems are then described as an alternative to reduce the size of the capacitor used in AC/DC/AC type systems. The problem of switching common-mode output voltage, present in both approaches, is discussed in more detail and a summary of the solutions reported is provided. Finally, matrix converter based open-end winding drive topologies, that are the topic of this dissertation, are introduced as a solution to the capacitor size and the switching common-mode output voltage.

1.1 AC/DC/AC voltage link drives

In modern electric drives, voltage source inverters (VSIs) are employed to generate a variable frequency AC voltage for fast and efficient control of electric machines. These VSIs are almost always two-level VSIs (2L-VSI) in low voltage applications ($< 1\,\mathrm{kV}$), whereas multilevel inverters are more common in medium voltage applications ($> 1\,\mathrm{kV}$) [1]. A front-end converter generates a DC voltage that is the input to the load-end VSI. Fig. 1.1 shows the architecture of a typical voltage link AC/DC/AC drive system. Active and passive components of the drive system are described below:

1. Voltage source inverter (VSI):

   (a) The VSI converts DC input voltage(s) to variable frequency pulse width

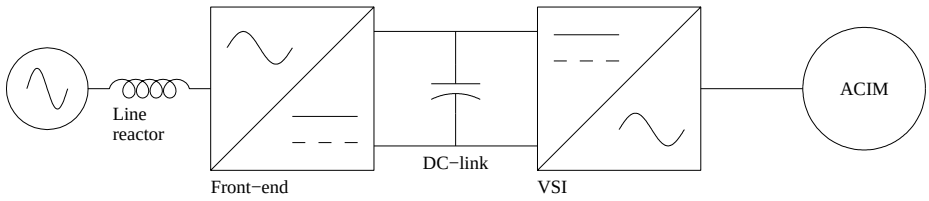


Figure 1.1: A voltage link AC/DC/AC drive for an AC induction motor (ACIM).

modulated (PWM) output voltages. Space vector PWM (SVPWM) and sine-triangle PWM with third harmonic injection are commonly used modulation techniques [2].

(b) The VSI could be a two-level VSI, common in low-voltage applications, or a three- or higher level inverter for higher voltages. For an n-level inverter, the DC bus is formed by $n-1$ series connected capacitors [1].

(c) The output voltage contains low- and high-frequency common-mode components. The high-frequency common-mode voltage causes electromagnetic interference (EMI) and bearing currents. Bearing currents have been conclusively linked to motor failure [3–10].

2. Following front-end converters are generally used for AC-DC conversion:

(a) Diode rectifier is the simplest and very commonly used front-end converter. Its main drawback is that it draws a large amount of current at non-triplen odd harmonics of the fundamental (5^{th}, 7^{th}, 11^{th} , 13^{th} ...) [11]. It also does not allow the power flow into the grid — therefore any regenerated energy must either be absorbed by the DC-link or expended across a braking resistor.

(b) Thyristor based front-ends with phase-shift transformers are used in higher power applications where the harmonic current drawn by the diode rectifiers is unacceptable. Such front-ends require line frequency transformers and tuned harmonic filters for harmonic elimination [11].

(c) VSIs can also be employed as front-end converters: VSIs allow power factor and DC-link voltage control with full regeneration capability. Additionally, these converters do not require line frequency transformers or tuned filters for acceptable current quality.

3. DC bus capacitor

   (a) In the case of a rectifier front-end, the DC bus capacitor is responsible for smoothing the sixth harmonic ripple voltage, as well as for providing low-voltage-ride-through (LVRT), and for absorbing the torque ripple from the machine.

   (b) In the case of a VSI front-end, the capacitor only filters a high-frequency current in the steady state. However, the decoupled converter control architecture necessitates that the DC bus rejects source and load disturbances i.e. the capacitor must provide LVRT and absorb the torque ripple.

   (c) The above considerations dictate that the DC bus capacitor should be quite large; the specific value is an application dependent engineering decision — a common rule of thumb is few tens of microfarads per unit load current. The capacitor design in VSI based drives requires careful optimization based on the capacitance per unit volume, ripple current rating, temperature rating, parasitic resistance and parasitic inductance offered by different capacitor technologies.

4. Input reactor/filter

   (a) Even though the grid input is somewhat inductive, the impedance offered is generally not enough to limit the harmonic current drawn by a rectifier type front-end. Therefore additional inductance is required at the rectifier AC input: the line reactors used to improve the quality of the input currents add to the weight, volume, and the cost of the system.

   (b) VSI front-ends generate an AC voltage that is connected to the grid through an inductor. Real and reactive power flow is controlled by varying the phase angle and the magnitude of this voltage relative to the grid. The inductor serves as a first-order filter that attenuates the PWM frequency component(s), hence limiting the harmonic current. While not necessarily as large as the inductor of a rectifier front-end, the input inductor is still ∼5–10%. Using a higher-order filter (e.g. LCL instead of merely L) can reduce the size and the cost of the inductors required [12].

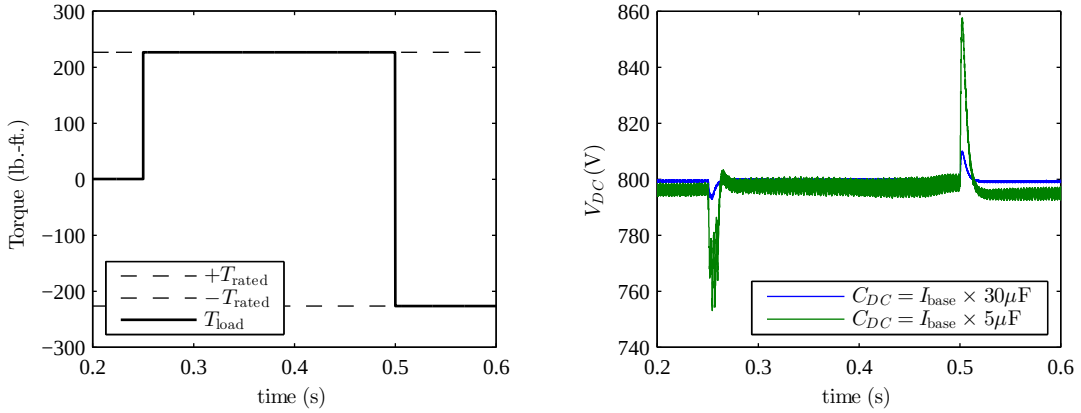
Overall, a VSI front-end offers the best regeneration capability and has the lowest input reactor requirements among the AC/DC/AC voltage link systems. There is no requirement of tuned filters either. In part due to now mature semiconductor technology, and in part due to the relative cost of copper as well as the size of additional passive components, the trend is toward using VSI front-ends. Such an arrangement where both converters, the load-end and the front-end, are VSIs, is also known as a back-to-back system. A back-to-back system will be treated as the state-of-the-art in this dissertation henceforth. The following issues, pertinent to back-to-back systems, and present in all VSI based solutions, deserve further discussion:

1.1.1 DC bus capacitor

As mentioned earlier, the DC bus capacitor needs to be sized to absorb the torque ripple from the machine and to meet the ride through specifications. If the ride through specifications are low to moderate, then the size of the capacitor is dictated by the task of absorbing the torque ripple. This is illustrated in Fig. 1.2: a back-to-back drive fed from a 480 V, 60 Hz, 3-phase AC voltage is driving a 460 V, 75 hp, 3-phase induction machine. The DC bus voltage is controlled to 800 V and the motor speed is controlled to 1800 rpm. In one case the DC bus capacitor is 30 μF per unit load current whereas in the other case it is 5 μF per unit load current. The load torque steps from no-load to rated torque T_{rated} at $t = 0.25\,\text{s}$, and again from T_{rated} to $-T_{\text{rated}}$ at $t = 0.50\,\text{s}$.

Both capacitors prove adequate in filtering the PWM frequency current at steady state; however, the DC voltage perturbation in response to torque perturbations is much higher in case of a small capacitor. Large swings in the DC bus voltage may trigger overvoltage protection or send the drive into unintended overmodulation. More serious consequences like device failure are also possible. To prevent undesirable phenomena due to torque transients, a common practice is to size the capacitor to be a few tens of microfarads per unit load current.

Film capacitors typically have high AC and DC voltage ratings, high ripple current ratings, low equivalent series resistance (ESR) and low equivalent series inductance (ESL). The life expectancy is very high and the failure mode is generally open-circuit [13]. Additional reliability is achieved by the self-healing property. The aforementioned features make film capacitors suitable for power electronic applications, and they are



(a) Load torque applied with the machine running at rated speed

(b) DC bus response to the applied torque for different capacitor values

Figure 1.2: Effect of torque ripple on the DC bus voltage for different capacitor sizes.

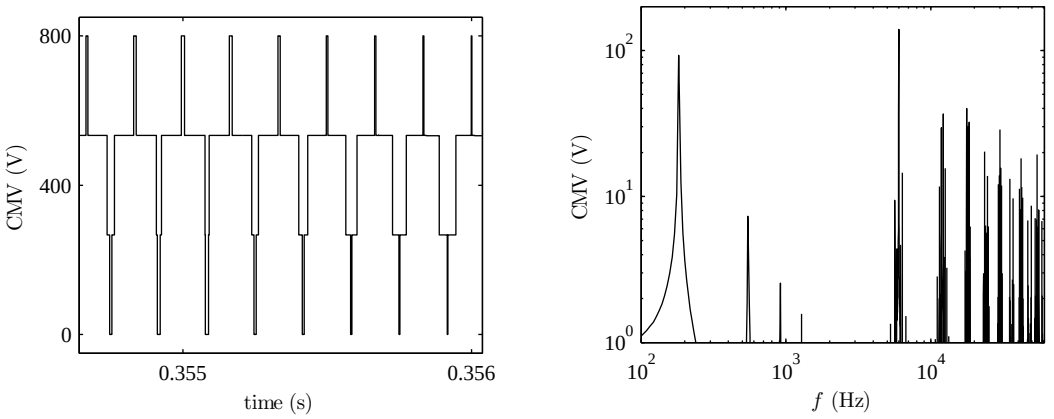
indeed extensively used, exclusively so in many applications.

However, the amount of capacitance required in VSI based motor drives is generally impractically large to be sourced entirely from film capacitors because of the volume, weight, and cost considerations. Therefore aluminum electrolytic capacitors are also used owing to their high capacitance density and low cost [13].

Ample experience with AC/DC/AC voltage link designs has identified the DC bus electrolytic capacitor as a weak link [14, 15] in an otherwise elegant architecture. However, no capacitor technology is currently available to completely replace the aluminum electrolytic capacitors in the VSI based drives without significantly increasing the cost and the physical size.

1.1.2 Common-mode voltage and bearing currents

The voltages synthesized by voltage source inverters (VSIs) contain low- and high-frequency common-mode components. The low-frequency common-mode components are injected on purpose to improve the DC bus utilization [2]. The high-frequency common-mode components, on the other hand, are simply a byproduct of the pulse width modulation (PWM). Fig. 1.3 shows the time and frequency domain plots of the common-mode voltage present in the output of a two-level VSI (2L-VSI).



(a) Common-mode voltage generated by a two-level VSI plotted against time. DC bus voltage is 800 V

(b) Spectrum of the common-mode voltage (a): low- and high-frequency components are seen

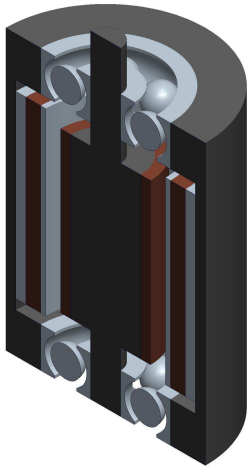
Figure 1.3: Common-mode voltage generated by a two-level VSI.

The common-mode components, by definition, do not contribute to the fundamental current. But the parasitic capacitances existing between the stator windings and the grounded frame (C_{ws}), between the stator windings and the rotor iron (C_{wr}), and between the rotor iron and the grounded frame (C_g) are excited by the high-frequency common-mode voltage (CMV). The parasitic paths are illustrated in Fig. 1.4.

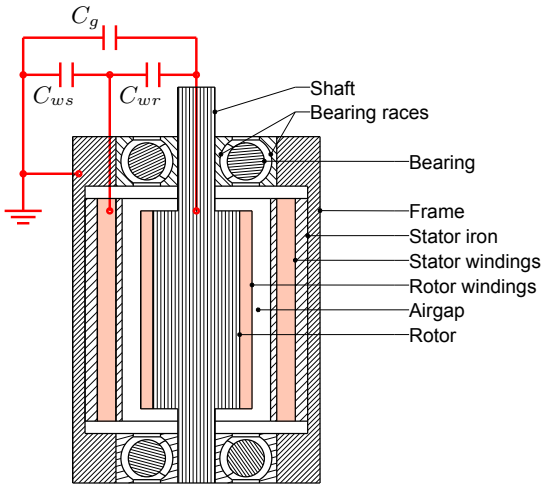
The high-frequency common-mode voltage causes several undesirable effects:

- In the common-mode equivalent circuit of Fig. 1.4(c), current flows from the motor terminals into the ground through all of the following paths [3]:
  - from the stator windings to the grounded frame via C_{ws}, the parasitic coupling between the stator windings and the frame;
  - from the stator windings to the grounded frame via C_{wr}, the parasitic coupling between the stator windings and the rotor iron, and C_g, the parasitic coupling between the rotor iron and the frame;
  - and from the stator windings to the grounded frame via C_{wr} and the bearings.

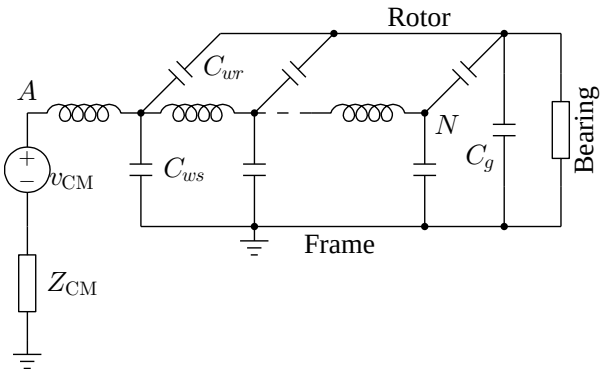
  The stray ground current flowing through the aforementioned paths causes electromagnetic interference (EMI).



(a) Simplified cutaway of an AC induction motor with exaggerated features



(b) Simplified cross-sectional view of an AC induction motor with stray capacitances shown



(c) Common-mode equivalent circuit of an AC induction motor [3]

Figure 1.4: Common-mode circuit of an AC induction motor.

- The finite impedance offered by the combination of C_g and the bearing, and the finite current through this impedance into the ground, cause a shaft voltage to develop:
  - Voltages as high as 40 V may develop [16, Section 31.4.4.3] raising safety concerns.
  - Sparks caused by shaft voltages may be detrimental in hazardous environments [17, 18].
- The bearing itself may appear as low to moderately resistive, or capacitive with a low breakdown voltage [4]:
  - Conduction-mode currents flow through the bearing when the common-mode voltage switches [3, 4].
  - Discharge-mode (EDM) currents flow through the bearing when the bearing lubricant film breaks down, discharging the shaft voltage across the bearing. These currents are typically larger than the conduction-mode bearing currents [4, 6].
  - Yet another type of bearing current, called the circulating bearing current, may flow as a byproduct of the common-mode currents discussed so far — this current, if it flows, circulates axially through the shaft and the frame via the bearings [6, 9].

According to [4], even with 60 Hz sinusoidal voltages, 30% of all motor failures can be attributed to bearing damage caused by bearing currents. A case study mentioned in [8] concludes that bearing damage related motor failures with modern PWM inverters could be as high as seven times the older six-step drives resulting in "increased downtime and depressed yields". Researchers from academia [3, 5, 6] and industry [4, 7, 8] have conclusively identified drive-induced bearing currents to be a leading cause of mechanical failure and the disruptive effect of these currents is acknowledged by National Electrical Manufacturers Association (NEMA) and American National Standards Institute (ANSI) [16].

1.2 Direct AC/AC converters and matrix converters

Direct AC/AC conversion is a VFD paradigm that does not employ an intermediate DC link. Cycloconverters [11] are direct AC/AC converters that synthesize a lower frequency AC waveform from a higher frequency AC waveform and are used for niche applications, especially at high power levels [19]. Direct matrix converters (DMCs) [20, 21] are a class of pulse width modulated (PWM) direct AC/AC converters in which four-quadrant switches are controlled based on a modulation matrix **M**:

$$\mathbf{v}_{\text{out}}^{*} = \mathbf{M}\,\mathbf{v}_{\text{in}} \tag{1.1}$$

Here $\mathbf{v}_{\text{out}}^{*}$ is the desired output voltage. Provided **M** exists, output voltage $v_{\text{out},j}$ is synthesized by applying input voltage $v_{\text{in},i}$ for M_{ij} duration of a sampling/switching interval over all i (PWM). Fig. 1.5 shows the block diagram of a direct matrix converter.

In this converter, the reactive elements are used only for filtering the PWM frequency. Furthermore, the inductor and the capacitor shown in Fig. 1.5 form a second-order filter, unlike a voltage link back-to-back converter system where the input inductor functions as a first-order filter (unless a higher order filter is explicitly included). Therefore, the reactive elements used in the direct matrix converter are potentially smaller than VSI based drives [22–24].

The modulation of direct matrix converters can also be considered in the space vector domain [25]. When modulated only using rotating vectors, the common-mode output voltage in a DMC is identically equal to zero. Therefore, DMCs present a low-passive and common-mode free alternative to VSI based drives. However, a poor voltage transfer ratio of 0.50 excludes rotating vector modulated DMCs from most applications. It should be noted that modulation using rotating vectors is equivalent to [20].

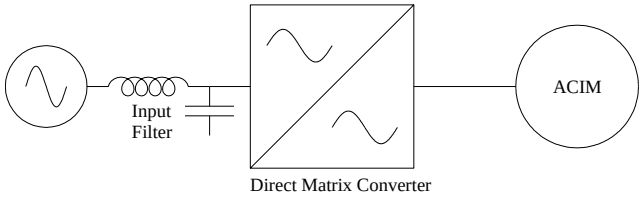


Figure 1.5: A direct matrix converter drive.

If stationary vectors are used for modulation, the voltage transfer ratio can be improved to 0.866 ($\sqrt{3}/2$) at the expense of generating low- and high-frequency common-mode output voltage. The injection of low-frequency common-mode voltage is explicit in [21]. The same input-output behavior can be realized by yet another class of converters known as indirect matrix converters (IMCs) shown in Fig. 1.6: this converter structure has distinct front-end and load-end parts connected at a soft link — this link is not a voltage/current stiff link, and ideally does not have any reactive components. Therefore, it does not decouple the grid-side and the load-side converters. Since the modulation philosophy of both, direct and indirect, PWM AC/AC converters is based on generating the output voltage from linear combinations of the instantaneous input voltages, as opposed to a decoupling DC voltage(s) derived from the input voltage, they are collectively known as matrix converters (MCs) that stand distinct from AC/DC/AC converters. References [25–29] provide comprehensive reviews of the advancements in matrix converters since their inception. The aforementioned publications also include discussions on converter topologies derived from the matrix converters of Figs. 1.5 and 1.6.

A voltage transfer ratio of $\sqrt{3}/2$ is achievable in direct and indirect matrix converters only at the cost of high-frequency common-mode voltage generation at the output. Input power factor can be controlled in both converters but the voltage transfer ratio is reduced below $\sqrt{3}/2$.

Henceforth in this dissertation, a direct matrix converter (DMC) modulated using the indirect transfer function approach of [25] would be referred to as conventional direct matrix converter (CDMC) shown in Fig. 1.7. Huber's indirect transfer function approach [25] treats the converter of Fig. 1.7 as a current source rectifier (CSR) and a voltage source inverter (VSI) connected at a hypothetical link. This hypothetical link

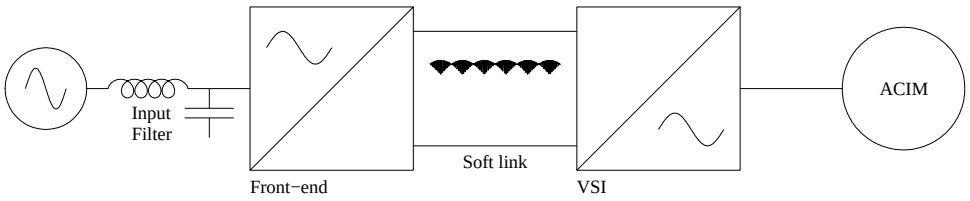


Figure 1.6: An indirect matrix converter drive.

can be made explicit resulting in a physical CSR-VSI structure of Fig. 1.6. This indirect matrix converter would be referred to as conventional indirect matrix converter (CIMC) in this dissertation. Conventional matrix converter (CMC) could mean either or both, CDMC and CIMC henceforth.

In summary, matrix converters, direct and indirect (CDMC and CIMC), are pulse width modulated AC/AC converters that require minimal reactive components. These converters have a maximum voltage transfer ratio of $\sqrt{3}/2$ at unity input power factor, and lower while operating at non-unity input power factor. Furthermore, these conventional matrix converters (CMCs) generate high-frequency common-mode output voltage.

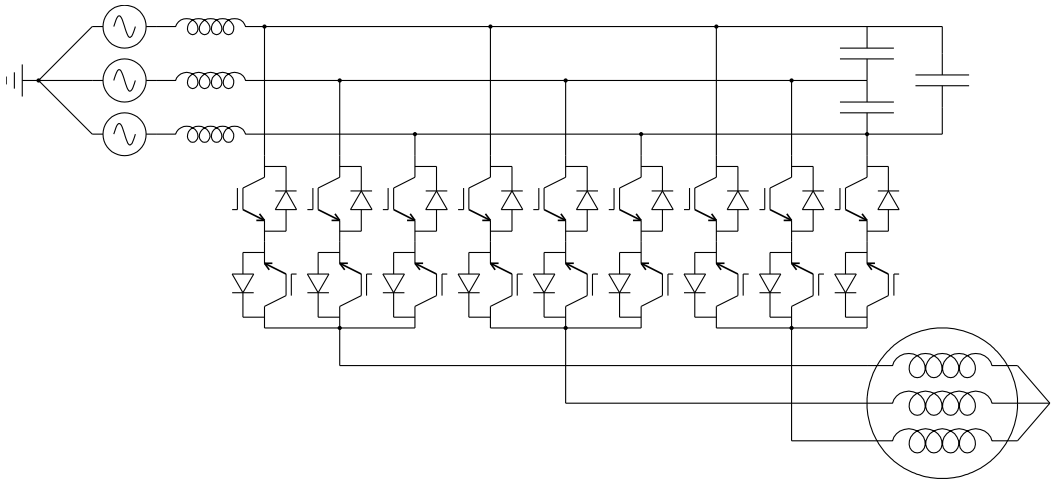


Figure 1.7: Conventional direct matrix converter (CDMC).

1.3 Common-mode and bearing current mitigation: state-of-the-art

A number of active and passive solutions have been studied and employed to mitigate the bearing currents or common-mode currents in general [8, 30, 31]. A simple solution is to add differential and/or common-mode impedance at the inverter output e.g. load reactors and common-mode chokes. Of course, such a solution entails additional components, and may even exacerbate the problem [8]. Shaft grounding brushes can

be used to provide a path to the currents that would otherwise flow through the bearings. On the other hand, a bearing insulation sleeve can be used to insulate the bearing from the frame. Whether an alternative conduction path is provided, or the existing conduction path is interrupted, the effectiveness of the solution is conditional upon periodic inspection and maintenance to ensure grounding integrity and/or the absence of contaminants which may not always be practical. Yet another method to interrupt the bearing currents is to use non-conductive ceramic bearings. The type of ceramic bearings that effectively interrupt these currents are expensive and may have long lead times. Furthermore, both, the insulating sleeve and the insulated ceramic bearings, do not eliminate the shaft voltage that could pose dangers to personnel and in hazardous environments. Unchecked shaft voltage may also cause bearing currents in the coupled instruments and loads. Conductive grease can mitigate the more harmful discharge-mode bearing currents; however, the conductive additive may separate at high speeds or cause unintended wearing [8, 30].

A particularly well performing passive solution is an electrostatic shielded induction motor (ESIM) [4] where an electrostatic shield of conductive material (copper) is applied between the stator windings and the rotor windings. This shield is grounded, same as the frame, effectively bypassing the distributed capacitance C_{wr} of Fig. 1.4(c). However, an ESIM is expensive and difficult to implement [8] and is not commercially available [30].

Active common-mode current elimination measures work in closed-loop to negate the common-mode voltage (CMV) generated by the power electronic converter. The generated CMV is sensed and a proportional, but opposing, common-mode voltage is applied such that no common-mode current can flow. Active cancelers [32] and compensators [33] with significant reduction in the EMI and the shaft voltage have been reported. Such techniques, however, employ linear amplifier circuits to generate the compensating CMV — this leads to losses and additional thermal management requirements. A dedicated power source for the active compensator may be required for higher DC-link voltages. Furthermore, a common-mode transformer is still required to impress the amplifier's output on the drive system's common-mode circuit.

All of the aforementioned solutions to address the problem of common-mode currents

require components in addition to the basic drive system. The best performing techniques are either non-standard and expensive and/or impose losses and thermal management requirements. Therefore, considerable research has been devoted to mitigating common-mode voltage at the PWM converter itself. Reduction in the common-mode voltage generated by the two-level inverter has been reported [34–37]. Compared to the standard 2L-VSI, a lower common-mode voltage is inherent to multilevel inverters [38]. Further mitigation in multilevel inverters [39, 40] has been demonstrated. Theoretically complete elimination of the common-mode voltages for multilevel inverters has also been demonstrated [41–44]. However, the strategies that provide complete elimination do so by using only a limited set of available vectors, compromising either, or both, the voltage transfer ratio and the output voltage harmonic distortion.

Research in conventional matrix converter modulation with the aim of mitigating CMV has also been reported [45–54]. It should be noted that these strategies only mitigate, not eliminate, the common-mode voltage. Additionally, the shortcomings of matrix converters against back-to-back VSIs remain.

Yet another approach to common-mode voltage elimination has been open-end winding (OE Wdg.) drives wherein the stator windings are supplied from both ends. Several VSI-derived implementations have been reported in the literature [55–59]. However, the VSI-derived OE Wdg. drives still require a large capacitor to maintain the DC-link voltage same as the conventional VSI based drives.

Gupta *et al.* demonstrated a direct matrix converter (DMC) based OE Wdg. drive [60–64] that eliminated common-mode output voltage, and did not require any large reactive components for operation. It also overcame the voltage transfer ratio and input power factor control limitation of conventional matrix converters. Due to its significant advantages, this idea has also received attention for driving generalized n-phase machines [65–69] wherein the machine can have an arbitrary number of phases.

The same functionality as a direct matrix converter based open-end winding drive can also be realized using an indirect matrix converter structure with some added advantages as described in the next section.

1.4 Matrix converter based open-end winding drives with common-mode elimination

In a drive system, a finite common-mode voltage results whenever the motor terminal voltages do not add to zero:

$$v_{\mathrm{CM}} = \frac{v_A + v_B + v_C}{3} \tag{1.2}$$

where A, B, C are the motor terminals and v_A, v_B, v_C are the motor terminal voltages. As described by (1.1), a matrix converter applies the input voltages at the load terminals according to a given modulation strategy. If the input voltages are balanced, and the set of the output voltages is equal to the set of the input voltages at all instants, then the output common-mode voltage is identically equal to zero.

1.4.1 Direct matrix converter based open-end winding drive with common-mode elimination

Fig. 1.8 shows the block diagram of the direct matrix converter based open-end winding (OE Wdg.) drive presented by Gupta *et al.* [60–64]. This drive consists of two direct matrix converters (DMCs) feeding the two sets of terminals of an open-end winding machine. The inductors and the capacitors form an LC filter to filter the input current such that the grid current is sinusoidal. The damping component(s) and the clamp circuits are not shown.

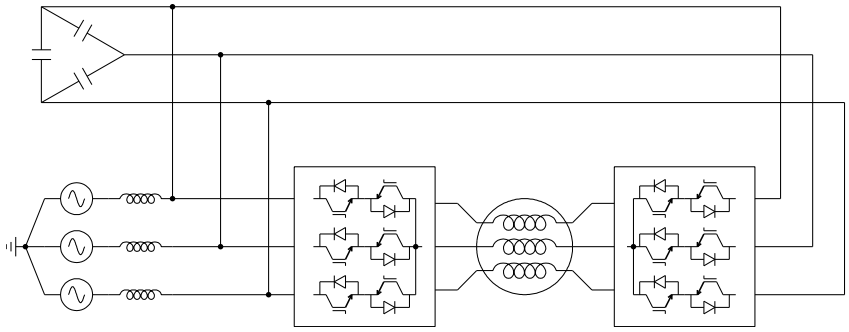


Figure 1.8: Block diagram of the direct matrix converter based open-end winding drive.

For an open-end winding drive, the definition of the common-mode voltage is extended to the two sets of motor terminals:

$$\begin{aligned} v_{\mathrm{CM}_1} &= \frac{v_{A_1} + v_{B_1} + v_{C_1}}{3} \\ v_{\mathrm{CM}_2} &= \frac{v_{A_2} + v_{B_2} + v_{C_2}}{3} \end{aligned} \tag{1.3}$$

where $\{A_1, B_1, C_1\}$ and $\{A_2, B_2, C_2\}$ are the two sets of motor terminals. The modulation strategy in [60–64] uses synchronously rotating vectors to eliminate the common-mode voltages $v_{\mathrm{CM}_1}, v_{\mathrm{CM}_2}$ defined above. Synchronously rotating vectors are the voltage vectors formed by the triplets $(v_a, v_b, v_c), (v_b, v_c, v_a), (v_c, v_a, v_b), (v_a, v_c, v_b), (v_c, v_b, v_a)$, and (v_b, v_a, v_c). These vectors rotate at $\pm\omega_i$ where ω_i is the input angular frequency. Without delving into the details of the modulation, it can still be seen that the common-mode voltage generated at a given set of terminals is zero if a synchronous vector is applied at that set of terminals. If exclusively synchronous vectors are used to synthesize the voltages at the two sets of terminals, the common-mode voltages $v_{\mathrm{CM}_1}, v_{\mathrm{CM}_2}$ are identically equal to zero.

The details of this DMC based OE Wdg. drive can be found in [60–64]. The major advantages of this approach are:

1. The common-mode output voltage is zero, thus eliminating a major cause of motor failure and other undesirable effects described in Section 1.1.2— an advantage over voltage source inverters (VSIs) and conventional matrix converters (CMCs).

2. The bulky and unreliable DC bus capacitor is removed from the system — an advantage over VSIs.

3. The voltage transfer ratio is increased to 1.50 — an advantage over CMCs.

4. The input power factor is controllable in a wide range without compromising the voltage transfer ratio — an advantage over CMCs

1.4.2 Indirect matrix converter based open-end winding drives with common-mode elimination

A direct matrix converter (DMC) connects the output phases *directly* to the input phases according to the modulation strategy being used. An indirect matrix converter connects

the output phases to the input phases at an intermediate link in the system — this link is the output of a front-end converter and also the input of a load-end converter(s).

There could be many indirect matrix converter circuit topologies and several are reviewed in references [27, 28]. This dissertation, however, only considers a limited set of circuits and modulation techniques that can eliminate the output common-mode voltage. The block diagrams of the indirect drives studied in this dissertation are shown in Fig. 1.9.

Let us consider the 'I-type' indirect matrix converter (IMC) based open-end winding (OE Wdg.) drive of Fig. 1.9(a). The circuit consists of three identical three-phase three-level bridges. These bridges are constructed using the well known neutral point clamped (NPC) three-level inverter structure, also known as the 'I-type' three-level inverter. One of the three converters serves as the front-end whereas the remaining two serve as the load-end converters. The inductors and the capacitors form a second-order LC filter to filter the current drawn by the grid. The damping network is not shown. The front-end converts the input voltages into intermediate link voltages; the load-end converters modulate the link voltages to drive the machine.

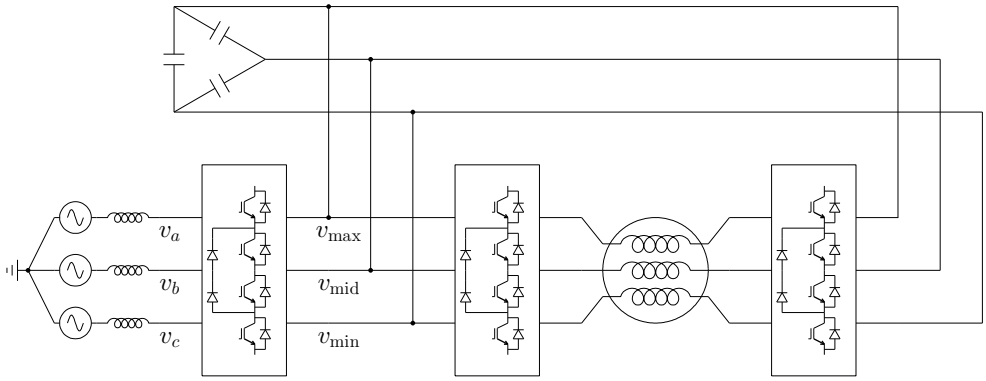
Let the input terminals be denoted by a, b, c and let v_a, v_b, v_c be the balanced input voltages. Let,

$$\begin{aligned} v_{\max} &= \max(v_a, v_b, v_c) \\ v_{\min} &= \min(v_a, v_b, v_c) \\ v_{\text{mid}} &= \underbrace{v_a + v_b + v_c}_{\equiv 0} - v_{\max} - v_{\min} \end{aligned} \tag{1.4}$$

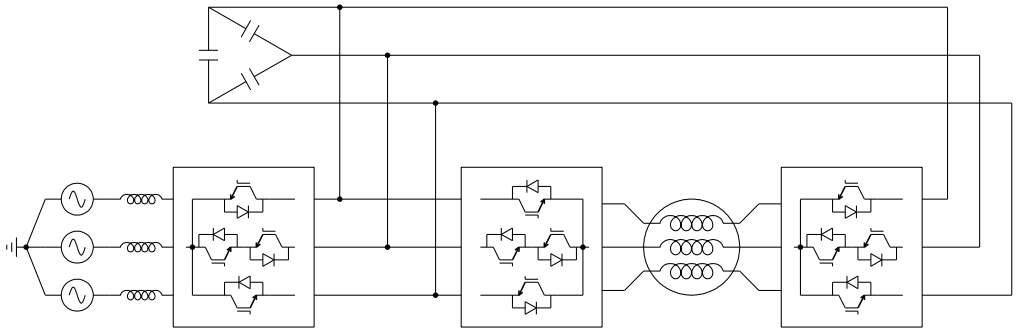
The front-end converter arranges the input voltages by their instantaneous value to output $v_{\max}, v_{\text{mid}}, v_{\min}$ at the link.

$$(v_a, v_b, v_c) \xrightarrow{\text{front-end}} (v_{\max}, v_{\text{mid}}, v_{\min}) \tag{1.5}$$

It is easy to see that $v_{\min} \leq v_{\text{mid}} \leq v_{\max}$, and that $v_{\max} + v_{\text{mid}} + v_{\min} = 0$. The load-end converters in Fig. 1.9(a) use the synchronous vectors formed by the triplets $(v_{\max}, v_{\text{mid}}, v_{\min}), (v_{\text{mid}}, v_{\min}, v_{\max}), (v_{\min}, v_{\max}, v_{\text{mid}}), (v_{\max}, v_{\min}, v_{\text{mid}}), (v_{\min}, v_{\text{mid}}, v_{\max})$, and $(v_{\text{mid}}, v_{\max}, v_{\min})$ to drive the machine. Since the set of the link voltages is also the set of the input voltages ($\{v_{\max}, v_{\text{mid}}, v_{\min}\} = \{v_a, v_b, v_c\}$) according to (1.4), the common-mode voltages $v_{\text{CM}_1}, v_{\text{CM}_2}$ are, once again, identically equal to zero.



(a) I-type indirect matrix converter based open-end winding drive



(b) T-type indirect matrix converter based open-end winding drive

Figure 1.9: Block diagrams of the indirect matrix converter based open-end winding drives considered: (a) I-type, and (b) T-type.

The drive of Fig. 1.9(a) uses the 'I-type' three-level inverter structure. Same functionality can also be realized using the less common 'T-type' structure (also marketed as 'mixed' NPC by at least one manufacturer), as shown in Fig. 1.9(b). This discussion is applicable to both circuit topologies of Fig. 1.9.

The detailed circuit and the operation of these drives will be described in the next chapter. However, it is important to note that the drives of Fig. 1.9 retain all the advantages of their direct matrix converter counterpart described in the previous subsection. In addition, the following advantages are unique to the indirect approach:

1. Intelligent commutation is possible without the need to sense current direction. In the DMC based drive, current direction sensing is necessary for optimal commutation, and it may be affected by noise [26].

2. No clamp circuit is necessary for protection or to aid commutation. In contrast, at least two three-phase fast recovery diode bridges and an additional DC capacitor are necessary in the DMC based OE Wdg. drive.

3. Power semiconductor devices never switch a voltage higher than 86.6% of the peak line-to-line voltage whereas in the DMC based drive, the maximum line-to-line voltage is switched by the semiconductor devices.

4. A low-voltage-ride-through (LVRT) strategy similar to the one proposed in [70] can be implemented for both, direct and indirect MC based OE Wdg. drives. However, in the case of the DMC based OE Wdg. drive, six additional IGBTs are required to construct the grid isolator of [70] whereas in the indirect implementation, the task of isolating the grid voltage sags can be performed by the front-end itself. Therefore, the IMC based OE Wdg. drives of Fig. 1.9 support natural LVRT integration.

This dissertation analyzes the direct and the indirect matrix converter based open-end winding drives described above. Comparison of the matrix converters topologies with each other, as well as with the state-of-the-art is included. The organization of this dissertation is now described.

1.5 Organization of this dissertation

This chapter laid out the motivation for the matrix converter based open-end winding drives. Elimination of the output common-mode voltage and the DC-link capacitor, and a practical voltage transfer ratio are the primary advantages anticipated. Results from the direct matrix converter based open-end winding drive have already been presented in the literature by other authors. The next chapter presents the experimental results demonstrating the operation of the two indirect matrix converter based open-end winding drives of Fig. 1.9. Before the experimental results are presented, the drive operation is discussed in detail and the equivalence of the direct and the indirect approaches from an input/output standpoint is established qualitatively. The advantages of the indirect approach over the direct approach are also discussed in detail. Analysis and design of a

third-order input current filter for all matrix converter based open-end winding drives is also included in Chapter 2.

Chapter 3 will identify the best performing matrix converter based open-end winding drive among the direct (Fig. 1.8) and the two indirect (Fig. 1.9) topologies. This will be accomplished by a comparison of the semiconductor losses, semiconductor requirements, passive element requirements, and input/output distortion over a wide range of operating points.

The best performing matrix converter based open-end winding drive identified in Chapter 3 will be compared against the state-of-the-art drive systems in Chapter 4. The criteria will include semiconductor requirements and losses, passive element requirements, and waveform quality. The comparison would be conducted over several operating points for an AC induction motor (ACIM) load. The findings and the contributions of this dissertation will be summarized in Chapter 5, which will also include recommendations and avenues for further research.

Chapter 2

Matrix converter based open-end winding drives: part 1

This chapter describes the development and the operation of matrix converter based open-end winding drives. Output voltage synthesis using space vector PWM (SVPWM), common-mode elimination, input power factor control, and the commutation strategy are discussed. Although the focus here is on the indirect topologies of Fig. 1.9, the ideas are equally applicable to the direct topology of Fig. 1.8 [60–64] as shown in a later section.

In addition to the semiconductor devices, the open-end winding drives discussed also require an input filter such that the current drawn from the grid is free of the high-frequency harmonics caused by the PWM operation. A second-order LC filter is commonly used in matrix converters. The design and optimization of a third-order filter with superior performance is also discussed in this chapter. This filter is applicable to all three topologies of Figs. 1.8 and 1.9.

2.1 Development of matrix converter based open-end winding drives for common-mode elimination

The early work of Alesina and Venturini [20] demonstrated a direct matrix converter where the set of the output voltages was always equal to the set of the input voltages,

i.e. the following conditions were met:

- No output phase is open (necessary for a typical motor/inductive load).
- No two input phases are connected to the same output phase (necessary for a typical ac voltage input).
- No two output phases are connected to the same input phase.

The first two conditions are fundamental for circuit operation whereas the last condition is a property of the modulation technique used for the three-phase-to-three-phase converter [20]. Combined, the three conditions can be stated as: every output phase is connected to a unique input phase at all times. Since balanced input voltages add to zero, so do the output voltages of such a converter. Therefore the common-mode voltage is, by definition, zero.

However, the maximum voltage transfer ratio of this converter was impractically low, and future work in matrix converter technology focused on the modulation techniques with a higher voltage transfer ratio.

Mohapatra and Mohan [60] recognized that a strategy such as described above can be used to eliminate the common-mode voltage, and that the machine could be run in an open-end winding (OE Wdg.) configuration from two direct matrix converters to improve the voltage transfer ratio. The possibility of an indirect implementation to reduce the switching losses was also identified [71]. If found feasible, these drives would eliminate the output common-mode voltage at practical voltage transfer ratios, as well as significantly reduce the reactive components required for operation.

Gupta developed the modulation strategy and the input power factor control strategy further and demonstrated a direct matrix converter based open-end winding drive with common-mode elimination [61–64] shown earlier in Fig. 1.8. Gupta further concluded that the modulation strategy for the direct matrix converter based drive could be tailored to the indirect implementation [64], and listed reduced switching losses and simplified protection clamp circuit as the possible advantages of the indirect implementation.

The present author published an analysis of the modulation technique for the indirect drive and also proposed a reduced four-step intelligent commutation scheme [72].

Experimental validation of a single-ended indirect matrix converter drive with common-mode elimination was provided in [73]. This drive was a reduced version of the drive in Fig. 1.9(a) and is shown in Fig. 2.1.

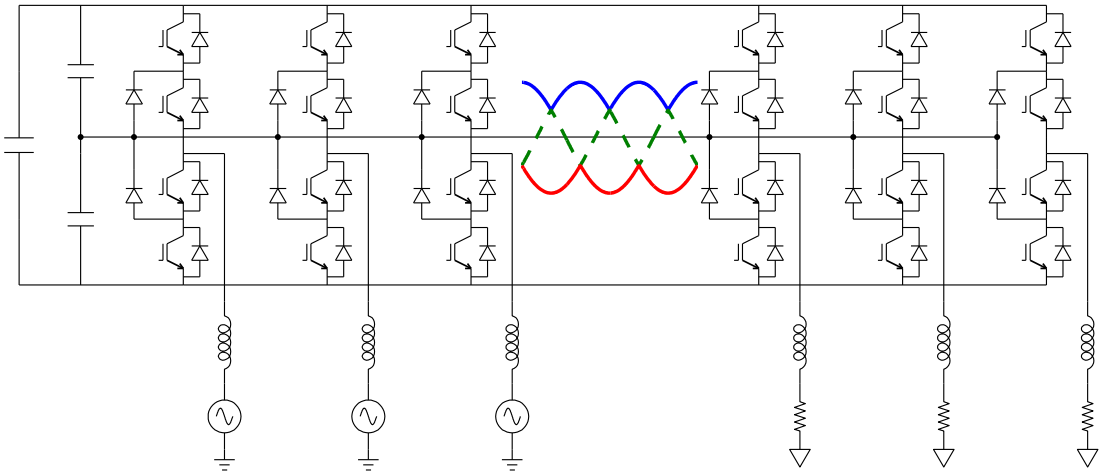


Figure 2.1: An indirect matrix converter based drive with common-mode elimination.

Although the voltage transfer ratio of the drive in Fig. 2.1 is limited to 0.50, it served to validate the feasibility of the indirect approach. In this chapter, the detailed theory of operation of the indirect matrix converter based open-end winding drives of Fig. 1.9 will be developed including the output voltage synthesis, input power factor control, details of the switching circuit and the commutation of the switches. The parallels with the direct matrix converter drive will be drawn qualitatively. A third-order filter for matrix converters will be proposed and optimized. The indirect approach and the filter design will be verified using experimental results, concluding the chapter.

2.2 Theory of operation

To facilitate the discussion, the space vector pulse width modulation (SVPWM) of a direct matrix converter (single-ended) with common-mode elimination is first described, followed by the slightly more complex modulation of the indirect matrix converter based open-end winding drives.

2.2.1 SVPWM of a direct matrix converter with common-mode elimination

Space vector transform maps a set of three-phase balanced quantities (typically voltages and currents) to a vector in the complex plane. Let f_{SV} be the space vector transform.

$$f_{\mathrm{SV}} : \mathbb{R}^3 \rightarrow \mathbb{C} \tag{2.1}$$

The value of the function f_{SV} corresponding to a given argument is typically called the space vector of the argument, or simply argument-space-vector. E.g. let $\{v_a, v_b, v_c\}$ be a set of three-phase balanced voltages at the input of a matrix converter, and let $f_{\mathrm{SV}}(v_a, v_b, v_c) = \vec{v}_{abc} \in \mathbb{C}$. $\vec{v}_{abc}$ is simply called the input voltage space vector. Equation (2.2) defines the space vector transform.

$$\vec{v}_{abc} = v_a + v_b\, e^{j2\pi/3} + v_c\, e^{-j2\pi/3} \tag{2.2}$$

Let the input voltages be,

$$\begin{aligned} v_a &= \widehat{v}_a \cos(\omega_i t) \\ v_b &= \widehat{v}_a \cos(\omega_i t - 2\pi/3) \\ v_c &= \widehat{v}_a \cos(\omega_i t + 2\pi/3) \end{aligned} \tag{2.3}$$

where $\widehat{v}_a$ is the amplitude of the input phase-to-neutral voltage and ω_i is the angular frequency. Substituting the above in (2.2) yields,

$$\begin{aligned} \vec{v}_{abc} &= 1.5\, \widehat{v}_a\, e^{j\omega_i t} \\ &= |\vec{v}_{abc}|\, e^{j\omega_i t} \end{aligned} \tag{2.4}$$

The vector $\vec{v}_{abc}$ has a constant magnitude and it rotates in the complex plane at a rotational speed of ω_i. The argument of the vector $\vec{v}_{abc}$ is the triplet (v_a, v_b, v_c). The vectors formed by the triplets (v_b, v_c, v_a) and (v_c, v_a, v_b) also rotate at a speed ω_i in the complex plane (positive sequence vectors). The vectors formed by triplets (v_a, v_c, v_b), (v_c, v_b, v_a), and (v_b, v_a, v_c), on the other hand, rotate at a speed $-\omega_i$ in the complex plane (negative sequence vectors). This is illustrated in Fig. 2.2. These vectors formed by the triplets of the set of the input voltages that rotate at $\pm\omega_i$ in the complex plane are called synchronous vectors henceforth. Unless otherwise mentioned, the modulation

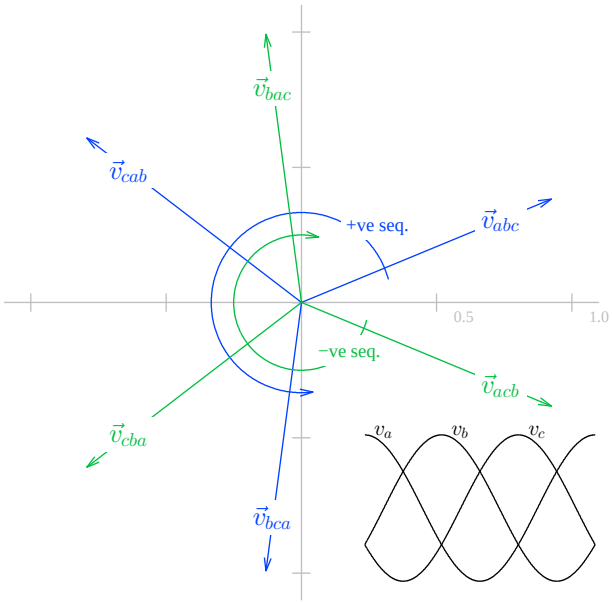


Figure 2.2: Positive sequence $(\vec{v}_{abc}, \vec{v}_{bca}, \vec{v}_{cab})$ and negative sequence $(\vec{v}_{acb}, \vec{v}_{cba}, \vec{v}_{bac})$ space vectors with magnitudes normalized by $|\vec{v}_{abc}|$.

of matrix converters considered in this dissertation uses only synchronous vectors so that common-mode elimination is achieved.

The purpose of a modulation strategy is to synthesize a set of balanced three-phase variable frequency output voltages. Let the desired output voltages be v_A^*, v_B^*, v_C^* with an amplitude $\widehat{v}_A^*$ and an angular frequency ω_o^*. Similar to the input, an output voltage space vector $\vec{v}_{ABC}^*$ can be defined:

$$\begin{aligned} \vec{v}_{ABC}^* &= 1.5\, \widehat{v}_A^*\, e^{j\omega_o^* t + \psi_o} \\ &= |\vec{v}_{ABC}^*|\, e^{j\omega_o^* t + \psi_o} \end{aligned} \tag{2.5}$$

where ψ_o is an arbitrary angle. In general, the output voltage amplitude and frequency will be controlled by the drive controller and the desired output voltage vector could simply be called $\vec{v}^*$. Either or both, the positive and the negative sequence vectors can be used for output voltage synthesis. For now, we will use only one set. Let $\{\vec{v}_1, \vec{v}_2, \vec{v}_3\}$ either be the set $\{\vec{v}_{abc}, \vec{v}_{bca}, \vec{v}_{cab}\}$ or the set $\{\vec{v}_{acb}, \vec{v}_{cba}, \vec{v}_{bac}\}$. Let $\lambda_1, \lambda_2, \lambda_3$ be such that $\sum_{1,2,3} \lambda_i = 1$, and $\lambda_i \in [0, 1]$ for all i. The desired voltage can be synthesized if λ_i could

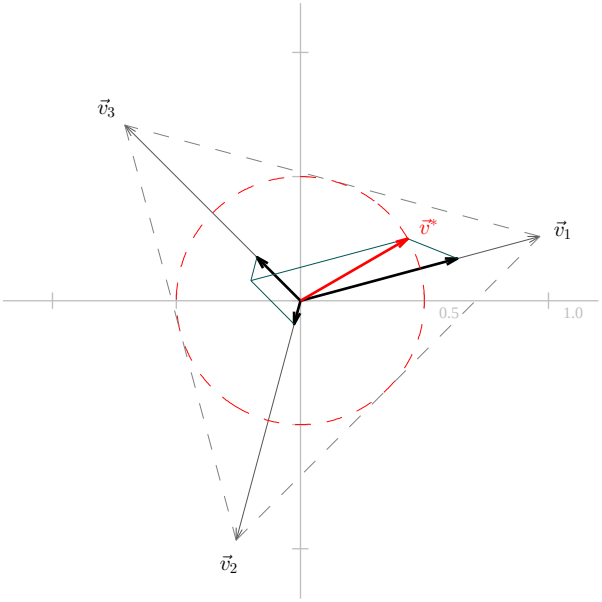


Figure 2.3: Output voltage synthesis.

be found such that:

$$\vec{v}^* = \lambda_1\vec{v}_1 + \lambda_2\vec{v}_2 + \lambda_3\vec{v}_3 \tag{2.6}$$

It is seen from (2.6) that $\vec{v}^*$ is a convex combination of the vectors $\vec{v}_1, \vec{v}_2, \vec{v}_3$. Therefore for λ_i to exist, $\vec{v}^*$ must lie within the convex hull of the vectors $\vec{v}_1, \vec{v}_2, \vec{v}_3$. This is illustrated in Fig. 2.3, where the dashed triangle is the convex hull of the vectors $\vec{v}_1, \vec{v}_2, \vec{v}_3$. Since $\angle\vec{v}^*$ is arbitrary, the maximum possible magnitude of $\vec{v}^*$ is the radius of the largest circle that can be inscribed within the dashed triangle (incircle) of Fig. 2.3. For space vectors separated by $2\pi/3$, the radius of such a circle is half the length of the space vectors. Therefore, the voltage transfer ratio is limited to 0.50, when using either the vectors $\{\vec{v}_{abc}, \vec{v}_{bca}, \vec{v}_{cab}\}$ or the vectors $\{\vec{v}_{acb}, \vec{v}_{cba}, \vec{v}_{bac}\}$ for output voltage synthesis.

Having established that using one set of vectors limits the voltage transfer ratio to 0.50, it is easy to see that using both sets simultaneously cannot extend this limit. The vector diagram in Fig. 2.2 is drawn at an arbitrary value of $\omega_i t$. The two sets of vectors coincide every π radians of the input voltage cycle. Since both sets of vectors become identical, it follows from the above discussion that the voltage transfer ratio cannot be increased beyond 0.50 at those instants. Therefore, in general, the voltage transfer ratio

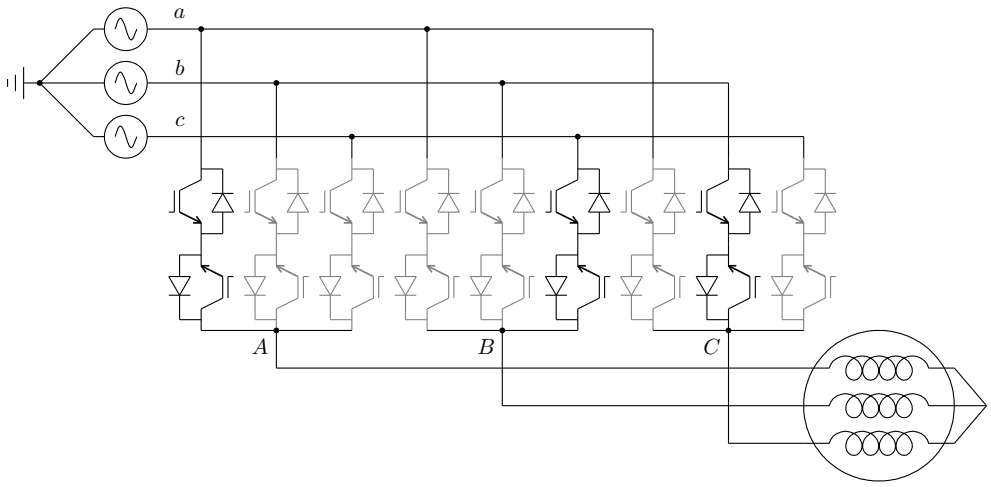


Figure 2.4: Applying vector $\vec{v}_{acb}$ at the output terminals — the dark IGBTs are turned ON and the grayed IGBTs are turned OFF.

cannot be increased beyond 0.50.

If the vector $\vec{v}^*$ lies within the incircle, then the output will be synthesized by applying vector $\vec{v}_i$ for λ_i fraction of some interval. A vector $\vec{v}_i$ is applied in this case by turning the appropriate switches ON, e.g. to apply the vector $\vec{v}_{acb}$, output phase A is connected to the input phase a, output phase B to the input phase c, and output phase C to the input phase b, by switching the appropriate switches ON and turning all the other switches OFF as shown in Fig. 2.4.

The equation (2.6) and the constraint that $\sum \lambda_i = 1$ can be rewritten as:

$$\lambda_1 \mathrm{Re}(\vec{v}_1) + \lambda_2 \mathrm{Re}(\vec{v}_2) + \lambda_3 \mathrm{Re}(\vec{v}_3) = \mathrm{Re}(\vec{v}^*) \tag{2.7}$$

$$\lambda_1 \mathrm{Im}(\vec{v}_1) + \lambda_2 \mathrm{Im}(\vec{v}_2) + \lambda_3 \mathrm{Im}(\vec{v}_3) = \mathrm{Im}(\vec{v}^*) \tag{2.8}$$

$$\lambda_1 + \lambda_2 + \lambda_3 = 1 \tag{2.9}$$

$$\Rightarrow \begin{pmatrix} \mathrm{Re}(\vec{v}_1) & \mathrm{Re}(\vec{v}_2) & \mathrm{Re}(\vec{v}_3) \\ \mathrm{Im}(\vec{v}_1) & \mathrm{Im}(\vec{v}_2) & \mathrm{Im}(\vec{v}_3) \\ 1 & 1 & 1 \end{pmatrix} \begin{pmatrix} \lambda_1 \\ \lambda_2 \\ \lambda_3 \end{pmatrix} = \begin{pmatrix} \mathrm{Re}(\vec{v}^*) \\ \mathrm{Im}(\vec{v}^*) \\ 1 \end{pmatrix} \tag{2.10}$$

λ_i can be calculated by solving (2.10).

Common-mode elimination principle

Assuming that $|\vec{v}^*| \leq 0.50\,|\vec{v}_{abc}|$, λ_i can be found by solving (2.10). The output voltage is synthesized by applying a vector $\vec{v}_i$ for λ_i fraction of some interval. This interval is the switching time period of the pulse width modulation and is decided based on semiconductor losses, control bandwidth and input/output harmonic distortion considerations.

During any λ_i fraction of the switching time period, the set of the output voltages is same as the set of the input voltages since every output phase is connected to a unique input phase ($\{v_A, v_B, v_C\} = \{v_a, v_b, v_c\}$). Since $\sum_{a,b,c} v_i = 0$, it follows that $\sum_{A,B,C} v_j = 0$ and therefore $v_{\mathrm{CM}} = 0$.

2.2.2 Indirect matrix converter based OE Wdg. drives: topologies

Structure of the direct matrix converter based open-end winding drive

The previous subsection described a direct matrix converter (DMC) based drive for driving wye- or delta-connected machines. The block diagram of the DMC based open-end winding drive is reproduced in Fig. 2.5 below. The main filter components are shown but the damping resistor and the protection clamp circuit are not shown here.

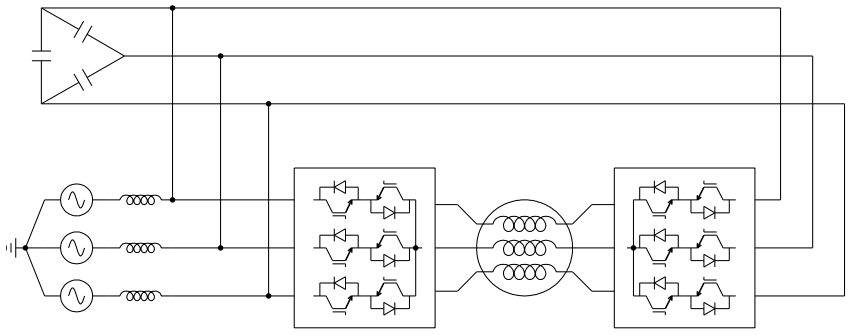


Figure 2.5: Block diagram of the direct matrix converter based open-end winding drive.

Let the machine terminals be called A_1, B_1, C_1 and A_2, B_2, C_2. Since the motor currents cannot be interrupted, every motor terminal is connected to an input phase at all times. In general, $v_j \lessgtr v_i$ for $j \in \{A_1, B_1, C_1, A_2, B_2, C_2\}$ and $i \in \{a, b, c\}$. Further, the motor currents ($:= i_A, i_B, i_C$) could be positive or negative. Therefore the switches connecting an input phase to an output phase must be able to block forward

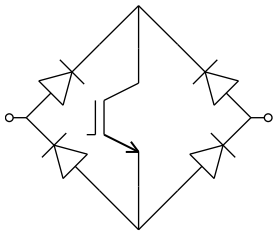


Figure 2.6: Four-quadrant switch using one IGBT and a diode bridge.

and reverse voltages, and must be able to conduct forward and reverse currents. Such a switch, that can block forward and reverse voltages and conduct forward and reverse currents is called a 'four-quadrant switch'. Fig. 2.6 shows a possible realization of a four-quadrant switch using an IGBT and a diode bridge.

Any current flowing through the switch of Fig. 2.6 has to overcome the ON-state voltage drop of three semiconductor devices. A four-quadrant switch formed by two common-emitter IGBTs and their freewheeling diodes offers lower conduction losses because the current flows though two semiconductor devices as opposed to three. Therefore the common-emitter IGBT is more common in matrix converter applications, although other realizations of a four-quadrant switch are also possible [26].

Fig. 2.7 shows the details of a typical DMC phase leg built with common-emitter IGBT four-quadrant switches. Output phase j can be connected to the input phase i using the switches $S_{ij,1}, S_{ij,2}$. Three such legs form the direct matrix converter of Fig. 1.7, which is redrawn in Fig. 2.4.

The clamping diodes $D_{\text{clamp},j}, D'_{\text{clamp},j}$ are also shown in Fig. 2.7. These diodes provide a path to the motor currents when all switches $S_{ij,1}, S_{ij,2}$ are turned OFF, intentionally or otherwise. In absence of the clamping diodes, interrupting the motor currents would cause detrimental overvoltages and destroy the power converter. Each motor terminal requires two clamping diodes capable of handling the rated load current and capable of blocking the peak line-to-line input voltage. The cathodes of the top clamping diodes are tied together and so are the anodes of the bottom clamping diodes. A DC capacitor, called the clamp capacitor C_{clamp} is connected across the cathodes of the top diodes and the anodes of the bottom diodes. A voltage equal to or greater than the peak of the input line-to-line voltage appears across C_{clamp} due to the boost converter

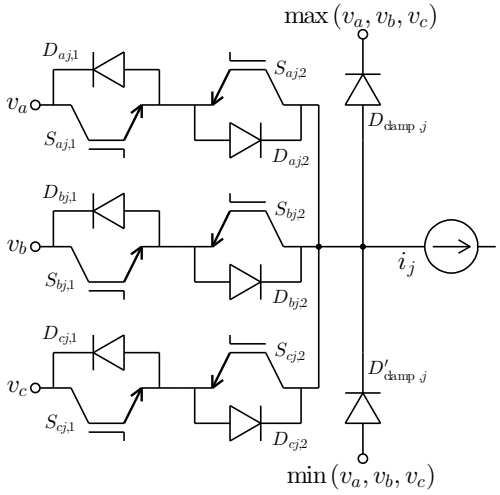


Figure 2.7: Phase leg of a direct matrix converter.

action of the power converter, clamp diodes, and the stator leakage inductances. Since the flow of energy into this capacitor is unidirectional, a discharging resistor R_{clamp} is required to limit the voltage, unless an energy recovery circuit is in place. Such a circuit can be used to power the auxiliary loads or to provide limited low-voltage-ride-through (LVRT) [22]. To avoid static power dissipation in the resistor R_{clamp}, it could be wired in series with a switch S_{clamp} that would turn ON only when the clamp capacitor voltage exceeds a certain limit. This configuration is similar to the brake IGBT and resistor used with VSIs.

The circuit diagram of the DMC OE Wdg. drive is shown in Fig. 2.8. The clamp circuit is not shown. The power processing and circuit protection requirements of this drive are summarized in Table 2.1. The filtering and instrumentation requirements would be discussed later.

Structure of the indirect matrix converter based open-end winding drives

A direct matrix converter based drive connects a given output phase directly to the appropriate input phase, as dictated by the modulation logic (e.g. application of the vector $\vec{v}_{acb}$ at the machine terminals shown in Fig. 2.4). An indirect matrix converter connects the output phases to the input phases at an intermediate link. This distinction

Component	Quantity	
IGBTs with freewheeling diodes	36	Semiconductors
Clamping diodes	12	
Clamp capacitor discharge switch	1	
Clamp capacitor	1	Passives
Clamp capacitor discharge resistor	1	

Table 2.1: Power processing and circuit protection requirements of a DMC based open-end winding drive.

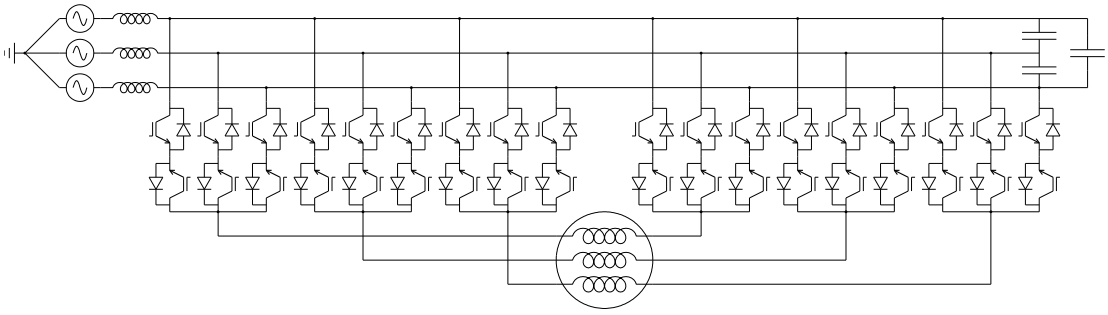


Figure 2.8: Circuit diagram of the direct matrix converter based open-end winding drive.

was described in Section 1.4.2 and the topologies of Figs. 1.9(a) and 1.9(b) were briefly discussed. Fig. 1.9(a) is reproduced in Fig. 2.9 below.

The drive of Fig. 2.9 has a front-end converter that generates the link voltages

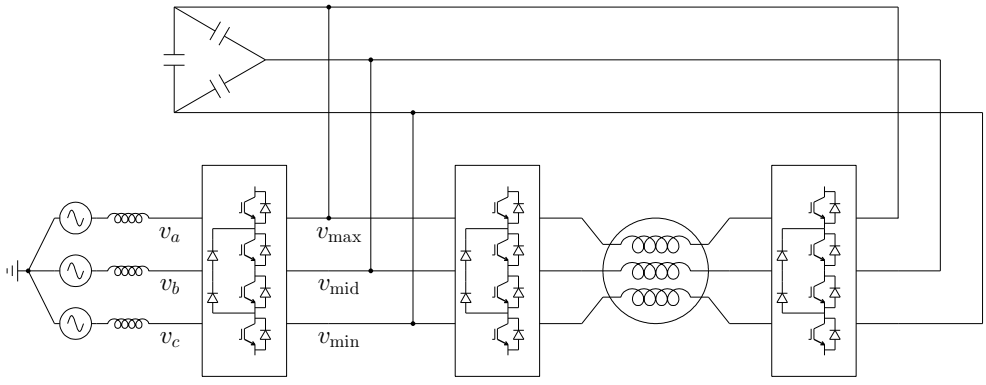


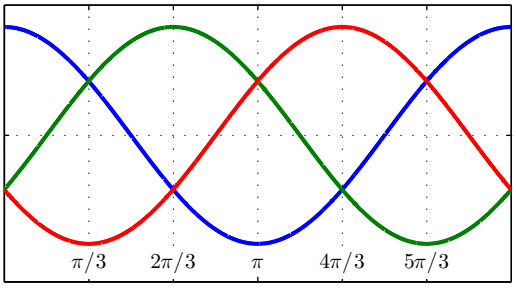
Figure 2.9: I-type indirect matrix converter based open-end winding drive.

$(v_{\max}, v_{\mathrm{mid}}, v_{\min})$ from the input voltages (v_a, v_b, v_c). Equations (1.4) and (1.5) describing the front-end's action are also reproduced below.

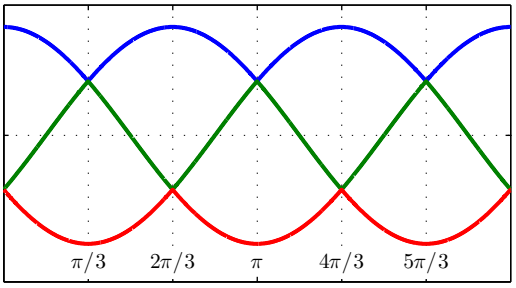
$$\begin{aligned} v_{\max} &= \max(v_a, v_b, v_c) \\ v_{\min} &= \min(v_a, v_b, v_c) \\ v_{\mathrm{mid}} &= \underbrace{v_a + v_b + v_c}_{\equiv 0} - v_{\max} - v_{\min} \\ (v_a, v_b, v_c) &\xrightarrow{\text{front-end}} (v_{\max}, v_{\mathrm{mid}}, v_{\min}) \end{aligned} \tag{2.11}$$

Operation of the front-end converter is illustrated in Fig. 2.10. It is seen that the front-end switches every $\pi/3$ radians (60°) of the input voltage cycle.

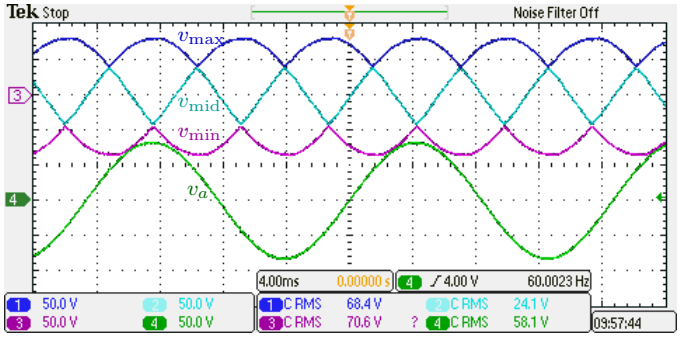
Henceforth, these 60° intervals would be called the 'sectors of the input voltage' or the 'input voltage sectors', or simply 'sectors' when the meaning is unambiguous. Within



(a) Balanced three-phase voltages are input to the front-end



(b) $v_{\max}, v_{\mathrm{mid}}, v_{\min}$ output by the front-end



(c) Front-end outputs $v_{\max}, v_{\mathrm{mid}}, v_{\min}$ with the input voltage v_a (bottom) for reference

Figure 2.10: Typical front-end (a) inputs and (b) outputs. (c) Experimental results for a 100 Volt, 60 Hz three-phase input.

a given sector, the mapping from the input voltages (v_a, v_b, v_c) to the link voltages $(v_{\max}, v_{\text{mid}}, v_{\min})$ is constant. The boundary between the sectors is marked by the zero crossings of the line-to-line voltages. Table 2.2 defines the input voltage sectors as a function of $\angle\vec{v}_{abc}$.

Within a sector, the set of link voltages $\{v_{\max}, v_{\text{mid}}, v_{\min}\}$ is a set of three-phase balanced voltages with the same amplitude as the input voltages v_a, v_b, v_c. If a given set of output voltages can be synthesized from the three-phase input, then the same set can also be synthesized from the link voltages. This idea is central to the adaptation of Gupta's modulation strategy [61–64] for direct matrix converter based open-end winding drive to the indirect matrix converter based open-end winding drives presented in this dissertation.

The load-end converters use the link voltages to generate a variable frequency output. The instantaneous load current could be positive or negative. However, the voltage at a given motor terminal cannot exceed $v_{\max}$; nor could it be lower than $v_{\min}$.

$$\begin{aligned} v_j &\leq v_{\max} \\ v_j &\lesseqgtr v_{\text{mid}} \\ v_j &\geq v_{\min} \\ i_j &\lesseqgtr 0 \end{aligned} \qquad j \in \{A_1, B_1, C_1, A_2, B_2, C_2\} \tag{2.12}$$

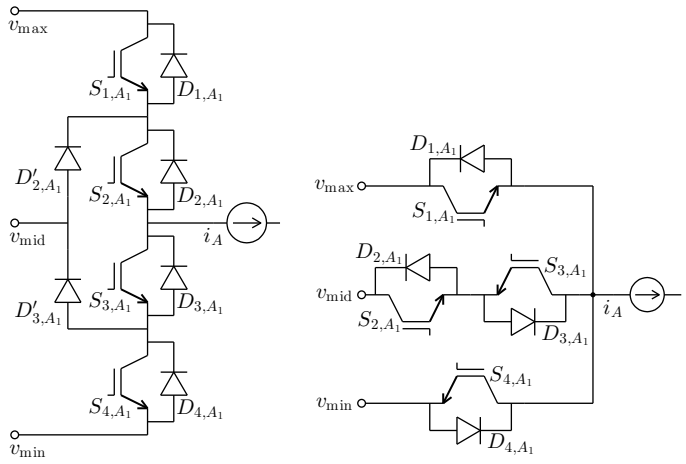
Therefore, the four-quadrant switch of Fig. 2.6 or Fig. 2.7 is not necessary to connect $v_{\max}$ and $v_{\min}$ to a given output phase. Furthermore, the conditions of (2.12) are also applicable to the input voltages. In fact, the circuit topology requirements of the front-end and the load-end converters are identical.

A three-level inverter generates a variable frequency AC output voltage by connecting an output phase to one of the three voltage inputs $V_{DC}, 0, -V_{DC}$ where $V_{DC} > 0$. The load current is an AC quantity and could be positive or negative. Since $v_{\min} \leq v_{\text{mid}} \leq v_{\max}$ and $i_i, i_j \lesseqgtr 0$ for all input and output phases, a three-level inverter structure

$\angle\vec{v}_{abc}$	$[0, \pi/3)$	$[\pi/3, 2\pi/3)$	$[2\pi/3, \pi)$	$[\pi, 4\pi/3)$	$[4\pi/3, 5\pi/3)$	$[5\pi/3, 2\pi)$
Sector	I	II	III	IV	V	VI

Table 2.2: Definition of the input voltage sectors.

can be used for the indirect matrix converter based open-end winding drive as shown in Fig. 2.11 for output phase A_1. Since the circuit topologies of Fig. 2.11 are sometimes called 'I-type' and 'T-type' in the context of three-level inverters, the corresponding indirect MC based OE Wdg. drives shall also be called 'I-type' and 'T-type'. The block diagram of the I-type indirect matrix converter based open-end winding drive is shown in Fig. 1.9(a) and again in Fig. 2.9; the block diagram of the T-type indirect matrix converter based open-end winding drive is shown in Fig. 1.9(b). The detailed circuit diagrams of the two topologies are shown in Fig. 2.12. Damping resistor and protection circuits are not shown.



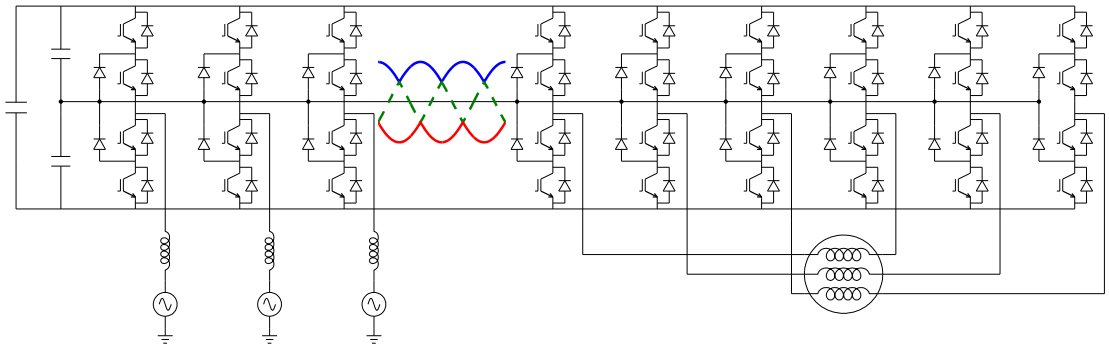
(a) I-type (b) T-type

Figure 2.11: Phase legs of the indirect matrix converter based open-end winding drives using (a) the I-type and (b) the T-type three-level inverter structures.

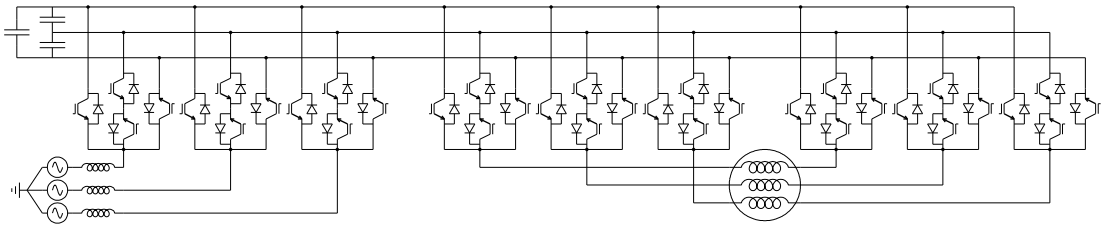
Clamp circuit elimination principle

The input currents of a matrix converter are sinusoidal only in an average sense — the instantaneous currents have a fundamental component at the input frequency and harmonics at the switching frequency and higher. To ensure a sinusoidal input current, a filter is included. A second order LC filter with some necessary damping is commonly used.

In the indirect drives of Fig. 2.12, the LC filter could have been connected at the circuit input same as the DMC OE Wdg. drive of Fig. 2.8. However, if the filter



(a) Circuit diagram of the I-type indirect matrix converter based open-end winding drive



(b) Circuit diagram of the T-type indirect matrix converter based open-end winding drive

Figure 2.12: Circuit diagrams of the indirect matrix converter based open-end winding drives (a) I-type and (b) T-type.

capacitors are placed at the link as shown in Figs. 1.9, 2.9 and 2.12, the freewheeling diodes of the IGBTs ensure a path for the motor currents into the filter capacitors in event of commutation failure. Therefore the freewheeling diodes also serve as clamping diodes and the filter capacitors also serve as the clamp capacitor. Furthermore, the voltage across the filter capacitors in the indirect case is dictated by the input voltage and the front-end, and energy can flow in and out of these capacitors, leaving no room for static losses in the clamp resistor (R_{clamp}) discussed earlier.

Hence a clamp circuit is no longer necessary in the indirect matrix converter based open-end winding drives. Of course, a brake IGBT and resistor should still be included to stop the motor and discharge the filter capacitors in the event of control failure. Tables 2.3 and 2.4 summarize the power processing and the circuit protection requirements of the indirect matrix converter based open-end winding drives. The filtering and instrumentation requirements would be discussed later.

Component	Quantity	
IGBTs with freewheeling diodes	36	Semiconductors
Neutral point clamping diodes	18	
Brake IGBT	1	
Brake resistor	1	Passives

Table 2.3: Power processing and circuit protection requirements of the I-type indirect MC based open-end winding drive.

Component	Quantity	
IGBTs with freewheeling diodes	36	Semiconductors
Brake IGBT	1	
Brake resistor	1	Passives

Table 2.4: Power processing and circuit protection requirements of the T-type indirect MC based open-end winding drive.

2.2.3 SVPWM of the indirect matrix converter based open-end winding drives for common-mode elimination

As explained in the last section, the front-end generates a set of balanced three-phase voltages. Similar to the input voltages, space vectors can be defined for the link voltages generated by the front-end:

$$\begin{aligned}
\vec{v}_{\mathrm{xdn}} &= v_{\max} + v_{\mathrm{mid}}\, e^{j2\pi/3} + v_{\min}\, e^{-j2\pi/3} \\
\vec{v}_{\mathrm{dnx}} &= v_{\mathrm{mid}} + v_{\min}\, e^{j2\pi/3} + v_{\max}\, e^{-j2\pi/3} \\
\vec{v}_{\mathrm{nxd}} &= v_{\min} + v_{\max}\, e^{j2\pi/3} + v_{\mathrm{mid}}\, e^{-j2\pi/3} \\
\vec{v}_{\mathrm{xnd}} &= v_{\max} + v_{\min}\, e^{j2\pi/3} + v_{\mathrm{mid}}\, e^{-j2\pi/3} \\
\vec{v}_{\mathrm{ndx}} &= v_{\min} + v_{\mathrm{mid}}\, e^{j2\pi/3} + v_{\max}\, e^{-j2\pi/3} \\
\vec{v}_{\mathrm{dxn}} &= v_{\mathrm{mid}} + v_{\max}\, e^{j2\pi/3} + v_{\min}\, e^{-j2\pi/3}
\end{aligned} \tag{2.13}$$

In the odd sectors (sectors I, III and V of Table 2.2), the voltages $(v_{\max}, v_{\mathrm{mid}}, v_{\min})$ appear as positive sequence and the set of vectors $\{\vec{v}_{\mathrm{xdn}}, \vec{v}_{\mathrm{dnx}}, \vec{v}_{\mathrm{nxd}}\}$ rotates at an speed ω_i; in the even sectors (II, IV, VI), the same voltages appear as negative sequence and the set $\{\vec{v}_{\mathrm{xdn}}, \vec{v}_{\mathrm{dnx}}, \vec{v}_{\mathrm{nxd}}\}$ rotates at an speed $-\omega_i$. This is illustrated in Fig. 2.13.

The set $\{\vec{v}_{\mathrm{xnd}}, \vec{v}_{\mathrm{ndx}}, \vec{v}_{\mathrm{dxn}}\}$ rotates opposite to the set $\{\vec{v}_{\mathrm{xdn}}, \vec{v}_{\mathrm{dnx}}, \vec{v}_{\mathrm{nxd}}\}$ in all sectors, appearing as positive sequence in even sectors and negative sequence in odd sectors.

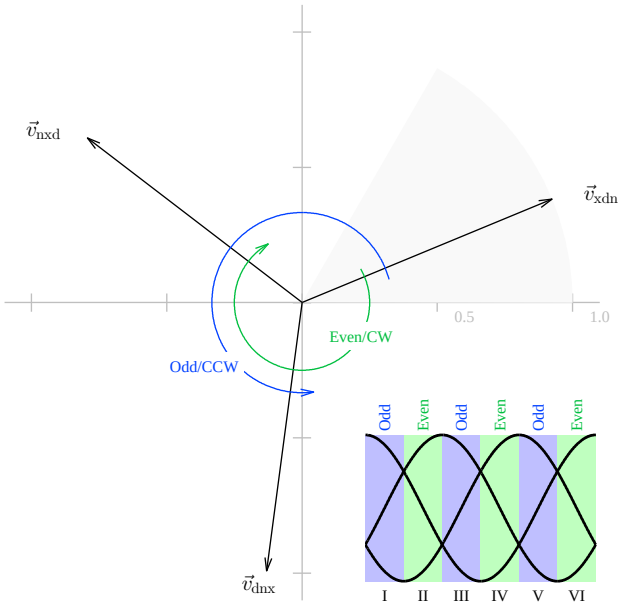


Figure 2.13: Vector diagram of the vectors $\{\vec{v}_{\text{xdn}}, \vec{v}_{\text{dnx}}, \vec{v}_{\text{nxd}}\}$.

Therefore, in all sectors, a set of counterclockwise rotating vectors and a set of clockwise rotating vectors is available for output voltage synthesis.

Let $\{\vec{v}_1, \vec{v}_2, \vec{v}_3\}$ be a set of vectors available for output voltage synthesis. $\{\vec{v}_1, \vec{v}_2, \vec{v}_3\}$ could either be $\{\vec{v}_{\text{xdn}}, \vec{v}_{\text{dnx}}, \vec{v}_{\text{nxd}}\}$, or $\{\vec{v}_{\text{xnd}}, \vec{v}_{\text{ndx}}, \vec{v}_{\text{dxn}}\}$. Although there is no restriction on using both sets of link voltage vectors, only one set will be considered first. Fig. 2.14 shows the vectors diagram of the vectors available for output voltage synthesis in the open-end winding drive. Vectors $\vec{v}_1, \vec{v}_2, \vec{v}_3$ are available at both ends of the machine. Since applying a vector $\vec{v}_i$ at one end and applying a vector $\vec{v}_j$ at the other end is equivalent to applying $\vec{v}_i - \vec{v}_j$, the vectors $\vec{v}_{1,1}, \vec{v}_{1,2}, \vec{v}_{1,3}, \vec{v}_{2,1}, \vec{v}_{2,2}, \vec{v}_{2,3}, \vec{v}_{3,1}, \vec{v}_{3,2}, \vec{v}_{3,3}$ are *effectively* available, where $\vec{v}_{ij}$ denotes $\vec{v}_i - \vec{v}_j$. The zero vectors $\vec{v}_{1,1}, \vec{v}_{2,2}, \vec{v}_{3,3}$ are not marked in Fig. 2.14.

The hexagon enclosing the vector diagram of Fig. 2.14 is the convex hull of the effective vectors $\vec{v}_{1,2}, \ldots$ These vectors have a magnitude $\sqrt{3}$ times the magnitude of the link voltage vectors $\vec{v}_{\text{xdn}}, \ldots$ and the radius of the incircle of the hexagon is 1.5. The magnitude of the link voltage vectors is equal to the magnitude of the input voltage vectors $\vec{v}_{abc}, \ldots$ — therefore an output voltage up to 1.5 times the input voltage can be

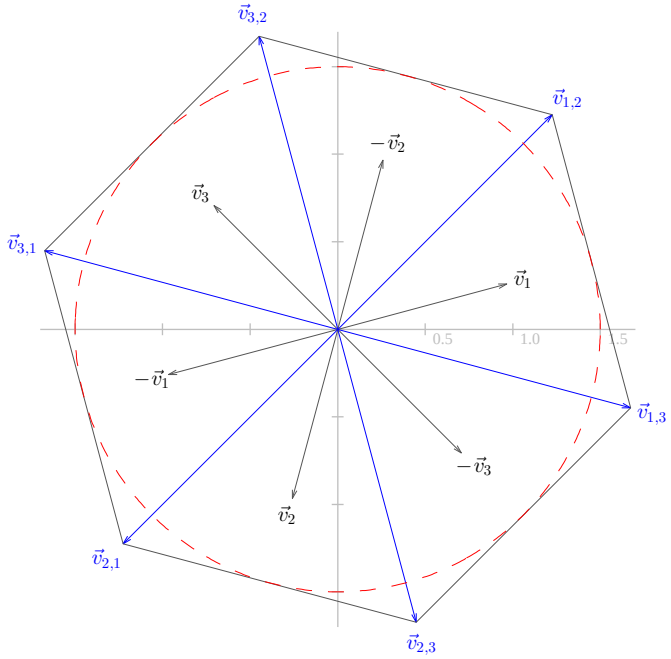


Figure 2.14: Vector diagram of the vectors available for output voltage synthesis.

synthesized.

Let the desired output voltage vector be $\vec{v}^*$. Let $\lambda_{11}, \lambda_{12}, \lambda_{13}$ and $\lambda_{21}, \lambda_{22}, \lambda_{23}$ be: $\sum_{1,2,3} \lambda_{1i} = 1, \sum_{1,2,3} \lambda_{2j} = 1$, and $\lambda_{1i}, \lambda_{2j} \in [0,1] \, \forall \, i, j \in \{1,2,3\}$.

$$\vec{v}^* = \underbrace{\lambda_{11}\vec{v}_1 + \lambda_{12}\vec{v}_2 + \lambda_{13}\vec{v}_3}_{=\vec{v}_{A_1B_1C_1}} - \underbrace{(\lambda_{21}\vec{v}_1 + \lambda_{22}\vec{v}_2 + \lambda_{23}\vec{v}_3)}_{=\vec{v}_{A_2B_2C_2}} \tag{2.14}$$

The decomposition of the above equation into real and imaginary parts yields two equations. The conditions that $\sum_{1,2,3} \lambda_{1i} = 1, \sum_{1,2,3} \lambda_{2j} = 1$, yield two more. Four equations are insufficient to uniquely determine all λ.

Let the target vector $\vec{v}^*$ lie in the $\pi/3$ sector[1] formed by the vectors $\vec{v}_{1,3}$ and $\vec{v}_{1,2}$, and the incircle of the hexagon in Fig. 2.14. $\vec{v}^*$ can be synthesized by a convex combination

[1]The sector in this case is different from the input voltage sector.

σ of the vectors $\vec{v}_{1,3}, \vec{v}_{1,2}$ and a zero vector:

$$\vec{v}^* = \sigma_1\vec{0} + \sigma_2\vec{v}_{1,2} + \sigma_3\vec{v}_{1,3} \tag{2.15}$$

$$= \sigma_1\vec{v}_1 + \sigma_2\vec{v}_1 + \sigma_3\vec{v}_1 - (\sigma_1\vec{v}_1 + \sigma_2\vec{v}_2 + \sigma_3\vec{v}_3) \tag{2.16}$$

$$= \vec{v}_1 - (\sigma_1\vec{v}_1 + \sigma_2\vec{v}_2 + \sigma_3\vec{v}_3) \tag{2.17}$$

The zero vector in (2.16) was chosen to be $\vec{v}_{1,1}$. This is equivalent to choosing $\lambda_{11} = 1, \lambda_{12} = 0, \lambda_{13} = 0$ in (2.14). The equation (2.17) can be solved for unique σ_i. Equation (2.17) further indicates that the modulation strategy will apply a constant vector $\vec{v}_1$ at the set of terminals A_1, B_1, C_1 and a combination of the vectors $\vec{v}_1, \vec{v}_2, \vec{v}_3$ at the other set of terminals A_2, B_2, C_2. The choice of zero vector in (2.16) eliminates the switching losses in the load-end converter feeding the set of terminals A_1, B_1, C_1. The synthesis of $\vec{v}^*$ is illustrated in Fig. 2.15.

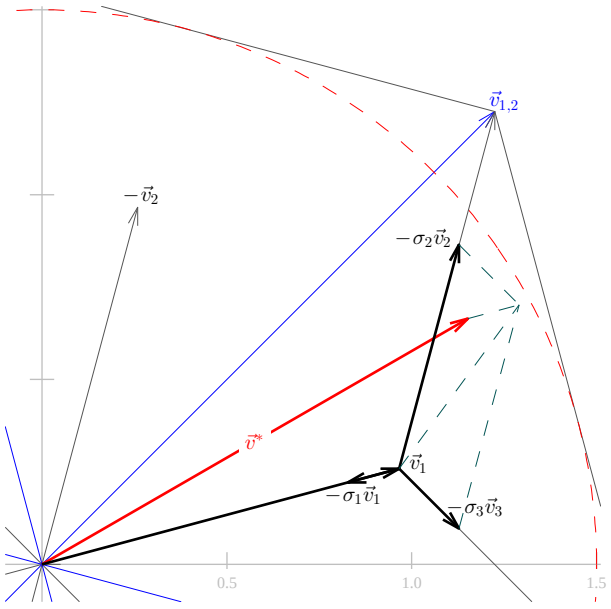


Figure 2.15: Synthesis of the output voltage vector.

The choice of the constant vector varies with the sectors[2], and between converters. For instance, if the vector $\vec{v}^*$ were to lie between the vectors $\vec{v}_{1,2}$ and $\vec{v}_{3,2}$, a constant vector $\vec{v}_2$ would be applied by the load-end converter at the set of terminals A_2, B_2, C_2. In general, if $\vec{v}^*$ lies in the convex hull of the origin and the adjacent vectors $\vec{v}_{ki}, \vec{v}_{kj}$, the vector $\vec{v}_k$ would be applied at terminals A_1, B_1, C_1 by that load-end converter for the entire time the vector $\vec{v}^*$ stays within that convex hull. Similarly, if $\vec{v}^*$ lies in the convex hull of the origin and the adjacent vectors $\vec{v}_{ik}, \vec{v}_{jk}$, the vector $\vec{v}_k$ would be applied at terminals A_2, B_2, C_2.

Power factor control

Let $(\vec{v}_1, \vec{v}_2, \vec{v}_3) = (\vec{v}_{\text{xdn}}, \vec{v}_{\text{dnx}}, \vec{v}_{\text{nxd}})$. Let $\vec{v}^*$ be as shown in Fig. 2.15. According to (2.17), $\vec{v}^*$ would be synthesized by applying the vector $\vec{v}_{\text{xdn}}$ at the terminals A_1, B_1, C_1, and synthesizing the vector $\vec{v}_{\text{xdn}} - \vec{v}^*$ at the terminals A_2, B_2, C_2 using a convex combination $(\sigma_1, \sigma_2, \sigma_3)$ of the vectors $(\vec{v}_{\text{xdn}}, \vec{v}_{\text{dnx}}, \vec{v}_{\text{nxd}})$.

$$\vec{v}^* = \vec{v}_{\text{xdn}} - (\sigma_1 \vec{v}_{\text{xdn}} + \sigma_2 \vec{v}_{\text{dnx}} + \sigma_3 \vec{v}_{\text{nxd}}) \tag{2.18}$$

Assume steady state. Let the equivalent load impedance be $|Z|\angle\phi_{\text{load}}$. Let the load currents be i_A, i_B, i_C. Further, let i_A, i_B, i_C be purely sinusoidal. Let $\vec{i}_{ABC} = f_{\text{SV}}(i_A, i_B, i_C)$ etc. Let $\bar{i}_{\text{x}}, \bar{i}_{\text{d}}, \bar{i}_{\text{n}}$ be the switching cycle averaged currents drawn by the load-end converters from the link. From (2.18),

$$\begin{aligned} \bar{i}_{\text{x}} &= i_A - (\sigma_1 i_A + \sigma_2 i_C + \sigma_3 i_B) \\ \bar{i}_{\text{d}} &= i_B - (\sigma_1 i_B + \sigma_2 i_A + \sigma_3 i_C) \\ \bar{i}_{\text{n}} &= i_C - (\sigma_1 i_C + \sigma_2 i_B + \sigma_3 i_A) \end{aligned} \tag{2.19}$$

Let $\vec{i}_{\text{xdn}} = f_{\text{SV}}(\bar{i}_{\text{x}}, \bar{i}_{\text{d}}, \bar{i}_{\text{n}})$. From a space vector transform on the equation above:

$$\vec{i}_{\text{xdn}} = \vec{i}_{ABC} - (\sigma_1 \vec{i}_{ABC} + \sigma_2 \vec{i}_{CAB} + \sigma_3 \vec{i}_{BCA}) \tag{2.20}$$

Substituting $\vec{i}_{BCA} = \vec{i}_{ABC} e^{-j2\pi/3}, \vec{i}_{CAB} = \vec{i}_{ABC} e^{j2\pi/3}$

$$\vec{i}_{\text{xdn}} = \vec{i}_{ABC}(1 - \sigma_1 - \sigma_2 e^{j2\pi/3} - \sigma_3 e^{-j2\pi/3}) \tag{2.21}$$

[2]The sector in this case is different from the input voltage sector.

Substituting $\vec{v}_{\text{dnx}} = \vec{v}_{\text{xdn}}e^{-j2\pi/3}, \vec{v}_{\text{nxd}} = \vec{v}_{\text{xdn}}e^{j2\pi/3}$ in (2.18)

$$\vec{v}^{*} = \vec{v}_{\text{xdn}}(1 - \sigma_1 - \sigma_2 e^{-j2\pi/3} - \sigma_3 e^{j2\pi/3}) \tag{2.22}$$

Substituting $\vec{i}_{ABC} = (\vec{v}^{*}\angle - \phi_{\text{load}})/|Z|$ in (2.21) and using (2.22)

$$\begin{aligned}
\vec{i}_{\text{xdn}} &= \frac{\vec{v}_{\text{xdn}}\angle - \phi_{\text{load}}}{|Z|} \times \\
&\qquad \left(1 - \sigma_1 - \sigma_2 e^{j2\pi/3} - \sigma_3 e^{-j2\pi/3}\right)\left(1 - \sigma_1 - \sigma_2 e^{-j2\pi/3} - \sigma_3 e^{j2\pi/3}\right) \\
&= \frac{\vec{v}_{\text{xdn}}\angle - \phi_{\text{load}}}{|Z|} \underbrace{\left|1 - \sigma_1 - \sigma_2 e^{-j2\pi/3} - \sigma_3 e^{j2\pi/3}\right|^2}_{\in \mathbb{R}} \\
&= \frac{\vec{v}_{\text{xdn}}\angle - \phi_{\text{load}}}{|Z|} \left(\frac{|\vec{v}^{*}|}{|\vec{v}_{\text{xdn}}|}\right)^2 \qquad \text{from (2.22)} \\
&= m^2 \, \frac{\vec{v}_{\text{xdn}}\angle - \phi_{\text{load}}}{|Z|}
\end{aligned} \tag{2.23}$$

where m is the voltage transfer ratio since $|\vec{v}_{\text{xdn}}| = |\vec{v}_{abc}|$. In the derivation above, the direction of rotation of the set $\{\vec{v}_{\text{xdn}}, \vec{v}_{\text{dnx}}, \vec{v}_{\text{nxd}}\}$ has not been invoked. Therefore, repeating the same derivation for the other set, $\{\vec{v}_{\text{xnd}}, \vec{v}_{\text{ndx}}, \vec{v}_{\text{dxn}}\}$, would yield identical result — for a lagging load, the link current vector $\vec{i}_{\text{xdn}}$ lags the link voltage vector $\vec{v}_{\text{xdn}}$ by the load power factor angle. The currents $\bar{i}_{\text{x}}, \bar{i}_{\text{d}}, \bar{i}_{\text{n}}$ can be calculated by the inverse space vector transform:

$$(\bar{i}_{\text{x}}, \bar{i}_{\text{d}}, \bar{i}_{\text{n}}) = f_{\text{SV}}^{-1}(\vec{i}_{\text{xdn}}) \tag{2.24}$$

Knowing the relationship between the input voltages and the link voltages, the link currents can be mapped to the input currents e.g. in sector I (of the input voltage), $(\bar{i}_a, \bar{i}_b, \bar{i}_c) = (\bar{i}_{\text{x}}, \bar{i}_{\text{d}}, \bar{i}_{\text{n}})$ whereas in sector II, $(\bar{i}_a, \bar{i}_b, \bar{i}_c) = (\bar{i}_{\text{d}}, \bar{i}_{\text{x}}, \bar{i}_{\text{n}})$, etc. Note that $\bar{i}_a, \bar{i}_b, \bar{i}_c$ are the switching cycle averaged input currents. The input voltages and switching cycle averaged currents are plotted in Fig. 2.16 for modulation using the set $\{\vec{v}_{\text{xdn}}, \vec{v}_{\text{dnx}}, \vec{v}_{\text{nxd}}\}$ for an inductive load.

The piecewise sinusoidal input current illustrates an important property of the modulation — in the odd sectors, where the voltages $(v_{\max}, v_{\text{mid}}, v_{\min})$ appear as positive sequence voltages, the input current lags the input voltage; in the even sectors where the voltages $(v_{\max}, v_{\text{mid}}, v_{\min})$ appear as negative sequence voltages, the input current

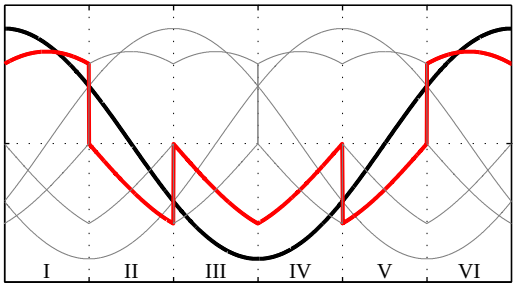


Figure 2.16: Input voltage and currents for modulation using the set $\{\vec{v}_{\text{xdn}}, \vec{v}_{\text{dnx}}, \vec{v}_{\text{nxd}}\}$ for an inductive load. Bold black waveform is the input voltage v_a, bold red waveform is the input current $\bar{i}_a$.

leads the input voltage. Therefore modulation using positive sequence link voltage results in an input power factor equal to the load power factor whereas modulation using negative sequence link voltages results in an input power factor opposite of the load power factor. Which triplet of voltages between $(v_{\text{max}}, v_{\text{mid}}, v_{\text{min}})$ and $(v_{\text{max}}, v_{\text{min}}, v_{\text{mid}})$ is positive sequence and which one is negative is determined by the instantaneous sector of the input voltage. Furthermore, to achieve power factor control at the input, both sets must be used. Let,

$$\mathbf{V}_{\text{pos}} = \begin{cases} [\vec{v}_{\text{xdn}}\ \vec{v}_{\text{dnx}}\ \vec{v}_{\text{nxd}}]^T & \text{odd sectors} \\ [\vec{v}_{\text{xnd}}\ \vec{v}_{\text{ndx}}\ \vec{v}_{\text{dxn}}]^T & \text{even sectors} \end{cases} \tag{2.25}$$

$$\mathbf{V}_{\text{neg}} = \begin{cases} [\vec{v}_{\text{xnd}}\ \vec{v}_{\text{dxn}}\ \vec{v}_{\text{ndx}}]^T & \text{odd sectors} \\ [\vec{v}_{\text{xnd}}\ \vec{v}_{\text{ndx}}\ \vec{v}_{\text{dxn}}]^T & \text{even sectors} \end{cases} \tag{2.26}$$

$$\mathbf{\Lambda}_{1,\text{pos}} = \begin{cases} [\lambda_{1,\text{xdn}}\ \lambda_{1,\text{dnx}}\ \lambda_{1,\text{nxd}}] & \text{odd sectors} \\ [\lambda_{1,\text{xnd}}\ \lambda_{1,\text{ndx}}\ \lambda_{1,\text{dnx}}] & \text{even sectors} \end{cases} \tag{2.27}$$

$$\mathbf{\Lambda}_{1,\text{neg}} = \begin{cases} [\lambda_{1,\text{xnd}}\ \lambda_{1,\text{dxn}}\ \lambda_{1,\text{ndx}}] & \text{odd sectors} \\ [\lambda_{1,\text{xdn}}\ \lambda_{1,\text{ndx}}\ \lambda_{1,\text{dnx}}] & \text{even sectors} \end{cases} \tag{2.28}$$

$$\mathbf{\Lambda}_{2,\text{pos}} = \begin{cases} [\lambda_{2,\text{xdn}}\ \lambda_{2,\text{dnx}}\ \lambda_{2,\text{nxd}}] & \text{odd sectors} \\ [\lambda_{2,\text{xnd}}\ \lambda_{2,\text{ndx}}\ \lambda_{2,\text{dnx}}] & \text{even sectors} \end{cases} \tag{2.29}$$

$$\mathbf{\Lambda}_{2,\text{neg}} = \begin{cases} [\lambda_{2,\text{xnd}}\ \lambda_{2,\text{dxn}}\ \lambda_{2,\text{ndx}}] & \text{odd sectors} \\ [\lambda_{2,\text{xdn}}\ \lambda_{2,\text{ndx}}\ \lambda_{2,\text{dnx}}] & \text{even sectors} \end{cases} \tag{2.30}$$

Let $\alpha : \alpha \in [0,1]$ be the power factor control parameter. The target output voltage vector $\vec{v}^*$ is synthesized using both sets of vectors:

$$\vec{v}^* = \alpha(\mathbf{\Lambda}_{1,\text{pos}} - \mathbf{\Lambda}_{2,\text{pos}})\mathbf{V}_{\text{pos}} + (1-\alpha)(\mathbf{\Lambda}_{1,\text{neg}} - \mathbf{\Lambda}_{2,\text{neg}})\mathbf{V}_{\text{neg}} \tag{2.31}$$

By varying α, it is possible to control the input power factor angle continuously in $[-\phi_{\text{load}}, +\phi_{\text{load}}]$ where ϕ_{load} is the load power factor angle.

Common-mode elimination principle

Equation (2.31) expresses the target output vector as a convex combination of all vectors available for synthesis. These vectors are $\{\vec{v}_{\text{xdn}}, \vec{v}_{\text{dnx}}, \vec{v}_{\text{nxd}}\}$ and $\{\vec{v}_{\text{xnd}}, \vec{v}_{\text{ndx}}, \vec{v}_{\text{dxn}}\}$. All of these vectors are obtained by space vector transform on triplets elements of which are $v_{\text{max}}, v_{\text{mid}}, v_{\text{min}}$. Since $\sum_{\text{max,mid,min}} v_i = 0$, it follows that $\sum_{A_1,B_1,C_1} v_i = 0$ and $\sum_{A_2,B_2,C_2} v_i = 0$.

Switching and commutation in the indirect matrix converter based open-end winding drives

A previous section described the modulation of the indirect matrix converter based open-end winding drives. The modulation strategy enables the calculation of the λ coefficients in (2.31) to synthesize the desired output vector $\vec{v}^*$. This section will discuss the derivation of the switching signals from the λ coefficients.

The power factor control parameter α in (2.31) is defined with respect to the positive and negative sequence voltages. A related parameter β could be defined for the set of vectors $\{\vec{v}_{\text{xdn}}, \ldots\}$

$$\beta = \begin{cases} \alpha & \text{input sectors I, III, V} \\ 1-\alpha & \text{input sectors II, IV, VI} \end{cases} \tag{2.32}$$

For input power factor control, the λ coefficients of the set $\{\vec{v}_{\text{xdn}}, \ldots\}$ will be scaled by β whereas the λ coefficients of the set $\{\vec{v}_{\text{xnd}}, \ldots\}$ will be scaled by $1-\beta$. Let the scaled coefficient be denoted by λ':

$$\lambda'_{1,i} = \begin{cases} \beta\lambda_{1,i} & \lambda_{1,i} \in \{\lambda_{1,\text{xdn}}, \lambda_{1,\text{dnx}}, \lambda_{1,\text{nxd}}\} \\ (1-\beta)\lambda_{1,i} & \lambda_{1,i} \in \{\lambda_{1,\text{xdn}}, \lambda_{1,\text{dnx}}, \lambda_{1,\text{nxd}}\} \end{cases} \tag{2.33}$$

The '1' in the subscript of λ' in (2.33) above denotes the first load-end converter [3] . $\lambda'_{2,i}$ can be defined similarly for the second load-end converter [4] . Let $\Lambda_{1,i}$ be the series of λ' coefficients for the first load-end converter:

$$\Lambda_{1,i} = \begin{cases} \lambda'_{1,\text{xdn}} & i = 1 \\ \lambda'_{1,\text{xdn}} + \lambda'_{1,\text{dnx}} & i = 2 \\ \lambda'_{1,\text{xdn}} + \lambda'_{1,\text{dnx}} + \lambda'_{1,\text{nxd}} & i = 3 \\ \lambda'_{1,\text{xdn}} + \lambda'_{1,\text{dnx}} + \lambda'_{1,\text{nxd}} + \lambda'_{1,\text{xnd}} & i = 4 \\ \lambda'_{1,\text{xdn}} + \lambda'_{1,\text{dnx}} + \lambda'_{1,\text{nxd}} + \lambda'_{1,\text{xnd}} + \lambda'_{1,\text{ndx}} & i = 5 \\ \lambda'_{1,\text{xdn}} + \lambda'_{1,\text{dnx}} + \lambda'_{1,\text{nxd}} + \lambda'_{1,\text{xnd}} + \lambda'_{1,\text{ndx}} + \lambda'_{1,\text{dxn}} & i = 6 \end{cases} \tag{2.34}$$

$\Lambda_{2,i}$ can be defined similarly. The continuous valued λ' coefficients represent the contribution of different link voltage vectors toward the desired output vector. These coefficients would be compared to a 'carrier' signal to generate Boolean signals. The pulse widths of the generated Boolean signals are proportional to the λ' coefficients they represent (pulse width modulation, PWM). The switches of the load end converters are controlled by these Boolean signals to apply the link voltage vectors at the load terminals. These PWM Boolean signals are also called 'duty cycles' in power electronics.

Within one period of the output voltage vector generation cycle, a given link voltage vector is applied at the load terminals for a duration equal to its λ' coefficient by passing the corresponding duty cycle signal to the pertinent switches. If the modulation is successful, the *average* vector applied in an output voltage generation period is equal to the desired output voltage vector.

Fig. 2.17 shows the series of the λ' coefficients of the first load-end converter: λ' coefficients are λ coefficients scaled by the power factor control parameter $\beta(\alpha, \text{sector})$ for some value of input and output voltages. Both sets of vectors are used, as would be the general case. The series of the λ' coefficients, $\Lambda_{1,i}$, is compared to a triangular carrier (c_{triangle}) to generate the cumulative duty cycle signals D. Consecutive cumulative duty cycle signals D are XORd to generate the individual duty cycle signals $\mathcal{D}$ that correspond

[3] The first load-end converter is the load-end converter that controls the voltage at the load terminals A_1, B_1, C_1

[4] The second load-end converter is the load-end converter that controls the voltage at the load terminals A_2, B_2, C_2

to the λ' coefficients of (2.33).

$$D(\Lambda_{1,i}) = \begin{cases} 0 & \Lambda_{1,i} \leq c_{\text{triangle}} \\ 1 & \Lambda_{1,i} > c_{\text{triangle}} \end{cases} \tag{2.35}$$

$$\mathcal{D}(\lambda'_{1,i}) = \begin{cases} D(\Lambda_{1,i}) & i = 1 \\ D(\Lambda_{1,i-1}) \oplus D(\Lambda_{1,i}) & i > 1 \end{cases} \tag{2.36}$$

To apply a link voltage vector $\vec{v}_{\text{xdn}}$ at the load terminals A_1, B_1, C_1, the switches of the first load-end converter must be controlled such that the output terminal A_1 gets connected to the link voltage v_{max}, the output terminal B_1 gets connected to the link voltage v_{mid}, and the output terminal C_1 gets connected to the link voltage v_{min}.

To apply a link voltage vector $\vec{v}_{\text{xnd}}$ at the load terminals A_1, B_1, C_1, the switches of the first load-end converter must be controlled such that the output terminal A_1 gets connected to the link voltage v_{max}, the output terminal B_1 gets connected to the link voltage v_{min}, and the output terminal C_1 gets connected to the link voltage v_{mid}.

Therefore, the switches in the first load-end converter that connect the load terminal A_1 to the link voltage v_{max} must be ON when the duty cycle signals $\mathcal{D}(\beta\lambda_{1,\text{xdn}})$ and $\mathcal{D}((1-\beta)\lambda_{1,\text{xnd}})$ are high. When the aforementioned signals are low, the output phase A_1 would be connected to a different link voltage. During those intervals, the switches must block the voltage appearing between the link voltage v_{max} and the load terminal A_1. Similar rules apply to other link and load terminals. Based on these rules, further duty cycle signals can be derived. E.g. for output phase A_1:

$$\begin{aligned} \mathcal{D}_{\text{x}A_1} &= \mathcal{D}(\beta\lambda_{1,\text{xdn}}) + \mathcal{D}((1-\beta)\lambda_{1,\text{xnd}}) \\ \mathcal{D}_{\text{d}A_1} &= \mathcal{D}(\beta\lambda_{1,\text{dnx}}) + \mathcal{D}((1-\beta)\lambda_{1,\text{dxn}}) \\ \mathcal{D}_{\text{n}A_1} &= \mathcal{D}(\beta\lambda_{1,\text{nxd}}) + \mathcal{D}((1-\beta)\lambda_{1,\text{ndx}}) \end{aligned} \tag{2.37}$$

The above signals are also shown in Fig. 2.17. Fifteen additional signals exist corresponding to the output phases B_1, C_1, A_1, B_2, C_2 and can be derived similarly. In these duty cycle signals, the information about the underlying vectors is obscured and they represent the relationship between an individual input (link) terminal and an individual output terminal.

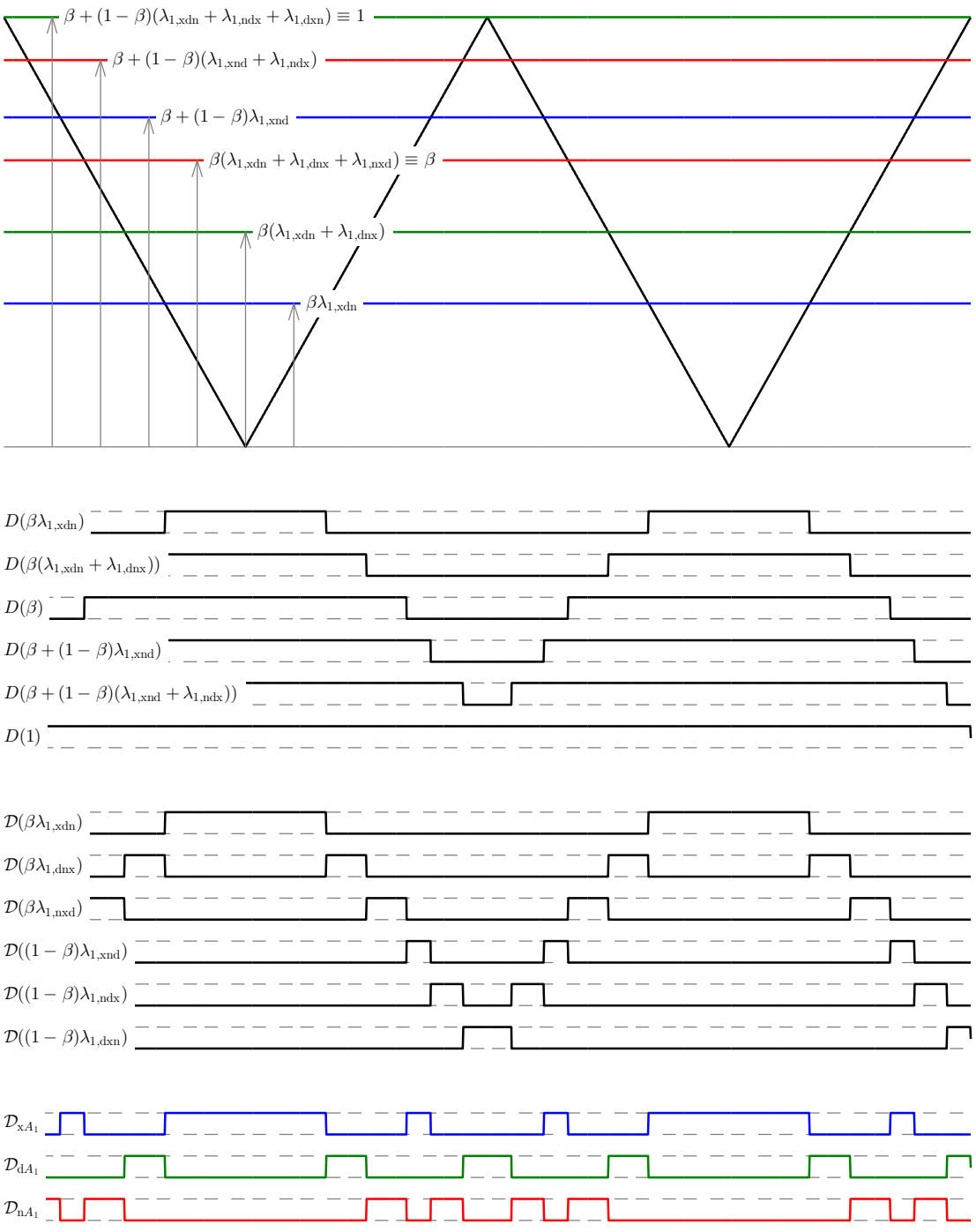
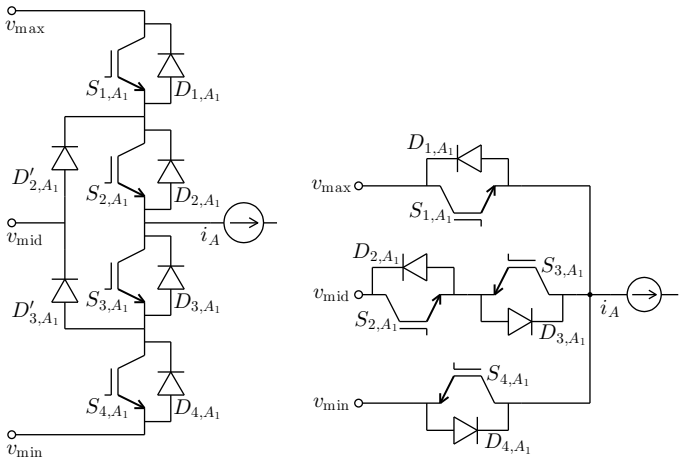


Figure 2.17: Switching signal generation.



(a) I-type (b) T-type

Figure 2.18: Phase legs of the indirect matrix converter based open-end winding drives using (a) the I-type and (b) the T-type three-level inverter structures.

The phase legs for both topologies of the indirect matrix converter based open-end winding drive are reproduced in Fig. 2.18. For the T-type topology in Fig. 2.18(b), the signal $\mathcal{D}_{\mathrm{x}A_1}$ can control the switch S_{1,A_1}, $\mathcal{D}_{\mathrm{d}A_1}$ can control the switches S_{2,A_1}, S_{3,A_1}, and $\mathcal{D}_{\mathrm{n}A_1}$ can control the switch S_{4,A_1}.

For the I-type topology of Fig. 2.18(a), however, to apply $v_{\max}$, both S_{1,A_1} and S_{2,A_1} need to be ON. Similarly to apply v_{mid}, S_{2,A_1} and S_{3,A_1} need to be ON; and to apply $v_{\min}$, S_{3,A_1} and S_{4,A_1} need to be ON. The switch S_{2,A_1} needs to be ON whenever a voltage $v_{\max}$ or a voltage v_{mid} needs to be applied, and it needs to be OFF whenever the third link voltage, $v_{\min}$ needs to be applied. The switch S_{4,A_1} needs to be ON only when $v_{\min}$ needs to be applied, and needs to be OFF at all other times. Therefore, S_{4,A_1} could be controlled directly from $\mathcal{D}_{\mathrm{n}A_1}$, and S_{2,A_1} can be controlled from the complementary signal $\overline{\mathcal{D}}_{\mathrm{n}A_1}$, where $\overline{\mathcal{D}}$ denotes logical negation of $\mathcal{D}$. Similar logic holds for S_{1,A_1} and S_{3,A_1}. The signals for this topology are therefore derived as:

$$\begin{aligned} q_{1,A_1} &= \mathcal{D}_{\mathrm{x}A_1} \\ q_{2,A_1} &= \overline{\mathcal{D}}_{\mathrm{n}A_1} \\ q_{3,A_1} &= \overline{\mathcal{D}}_{\mathrm{x}A_1} \\ q_{4,A_1} &= \mathcal{D}_{\mathrm{n}A_1} \end{aligned} \tag{2.38}$$

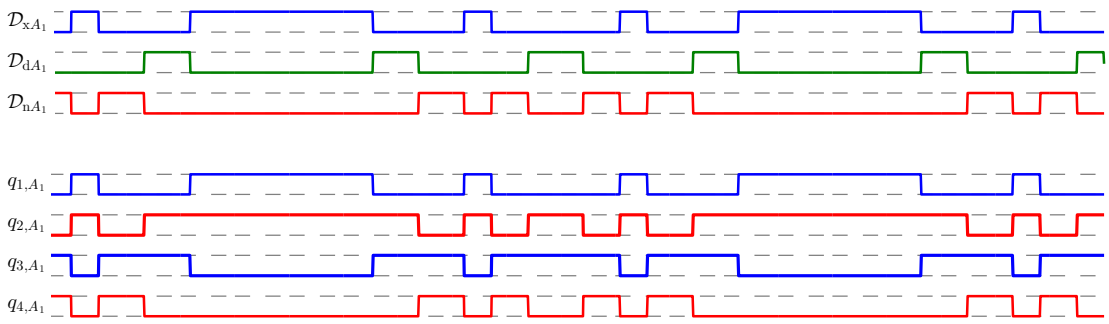


Figure 2.19: Switching signals for the I-type drive.

The signals defined above are shown in Fig. 2.19.

Commutation of the current

Let us now consider the commutation of the current at switching transitions. Let the output A_1 initially be connected to v_{max} (Fig. 2.20(a)) and finally to v_{mid} (Fig. 2.20(b)). The devices that are ON [5] are shown in black and the devices that are OFF are grayed out in Fig. 2.20. Let the current i_A be positive at the switching transition considered.

During the commutation, S_{1,A_1} is turned OFF first and then S_{3,A_1} is turned ON. Although the transitions seem simultaneous in the signals of Fig. 2.19, some delay is necessary to account for the finite switching times of the semiconductor switches. Upon turning S_{1,A_1} OFF, the diode D'_{2,A_1} turns ON naturally and the voltage v_{mid} appears at the output terminal. Had i_A been negative, the current would have continued to flow into the v_{max} terminal until S_{3,A_1} was turned ON. The intended voltage v_{mid} would have appeared at the output terminal after some small delay.

If the same process is considered in the T-type phase leg of Fig. 2.18(b) for $i_A > 0$, it is seen that in the duration between the turning OFF of S_{1,A_1} and the turning ON of S_{2,A_1} and S_{3,A_1}, the current would have been sourced out of the terminal v_{min} resulting in an unintended voltage at the output. While the period for which this unintended voltage would have appeared is small enough to have little, but finite, contribution to

[5] Some latitude is requested from the reader since ON/OFF behavior of diodes is not controllable and the gray or black color is assigned to the diodes based on whether they would conduct for $i_A \lesseqgtr 0$.

the output voltage distortion, a more important consideration is the switching loss in the diode D_{4,A_1}: upon the turn ON of S_{2,A_1} and S_{3,A_1}, the diode D_{4,A_1} that was conducting only to provide a path to the load current would get reverse biased and turn OFF. This turn OFF would be accompanied by reverse recovery losses in D_{4,A_1}.

However, if the signals $q_{1,A_1}\ldots$ (Fig. 2.19 and (2.38)) were to be used for the T-type topology as well, the application of an unintended voltage at the output and the associated reverse recovery losses would be eliminated since D_{4,A_1} would never turn ON.

Such commutation where the current commutates from the outgoing device *directly* to the incoming device is called intelligent commutation. It is inherent to two- and three-level inverters. Since the indirect matrix converter based OE Wdg. drives discussed in this dissertation use a three-level inverter structure, intelligent commutation is achieved by simply by using the switching signals derived in (2.38) — no knowledge of current direction is necessary; nor is a clamp circuit required to provide an alternative path to the motor currents.

On the other hand, to achieve intelligent commutation in direct matrix converters, also known as four-step commutation in their context, the direction of the current needs to be known. The determination of current direction is prone to noise [26] and a clamp circuit needs to be added to provide a path to the load currents in case of unintended

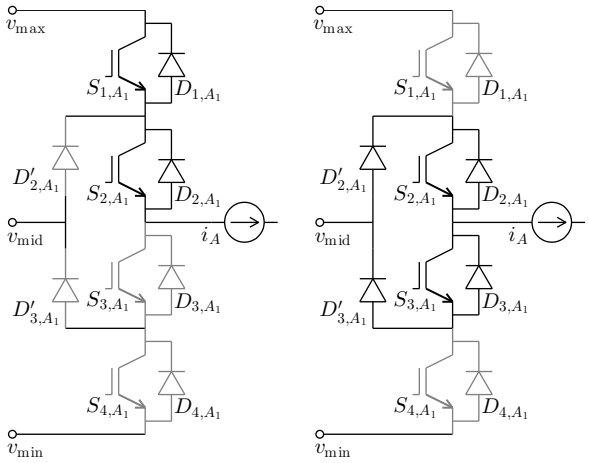


Figure 2.20: Commutation in the I-type topology.

disruption. The clamp circuit adds more components to the system. Furthermore, any operation of the clamp circuit is followed by reverse recovery losses in clamping diodes when normal operation is resumed.

Minimizing the switching losses and device voltage stress

In the Fig. 2.17, a triangular carrier was used and the link voltage vectors were applied at the output terminals A_1, B_1, C_1 in the following sequence:

$$\vec{v}_{\mathrm{xdn}}, \vec{v}_{\mathrm{dnx}}, \vec{v}_{\mathrm{nxd}}, \vec{v}_{\mathrm{xnd}}, \vec{v}_{\mathrm{ndx}}, \vec{v}_{\mathrm{dxn}}, \vec{v}_{\mathrm{dxn}}, \vec{v}_{\mathrm{ndx}}, \vec{v}_{\mathrm{xnd}}, \vec{v}_{\mathrm{nxd}}, \vec{v}_{\mathrm{dnx}}, \vec{v}_{\mathrm{xdn}}, \ldots$$

Other sequences are possible that minimize the number of switching transitions. Two such sequences are shown in Table 2.5 alongside the sequence above. The vectors are represented by the subscript and the $\vec{v}$ symbol is dropped. The two switching sequences that result in the least number of transitions are also illustrated in Fig. 2.21. T_s is the output voltage synthesis period and would be (somewhat loosely) called switching time period henceforth.

Between the two switching sequences identified in Table 2.5 and Fig. 2.21, the following sequence

A_1	B_1	C_1	A_1	B_1	C_1	A_1	B_1	C_1
x	d	n	x	d	n	x	d	n
d	n	x	x	n	d	x	n	d
n	x	d	d	n	x	d	n	x
x	n	d	n	d	x	d	x	n
n	d	x	n	x	d	n	x	d
d	x	n	d	x	n	n	d	x
d	x	n	d	x	n	n	d	x
n	d	x	n	x	d	n	x	d
x	n	d	n	d	x	d	x	n
n	x	d	d	n	x	d	n	x
d	n	x	x	n	d	x	n	d
x	d	n	x	d	n	x	d	n
28 transitions (Fig. 2.17)			20 transitions (Fig. 2.21(a))			20 transitions (Fig. 2.21(b))		

Table 2.5: Vector sequences possible in the indirect drives.

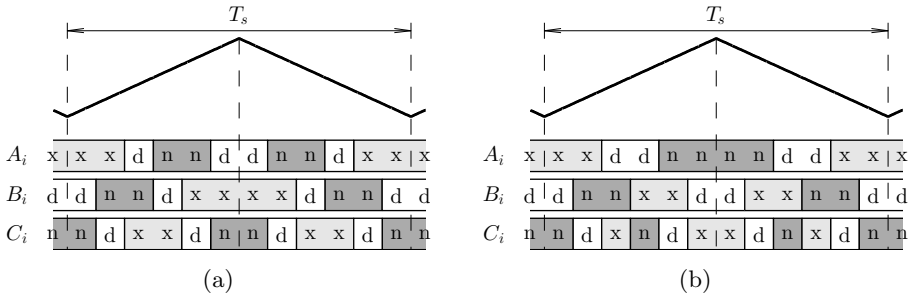


Figure 2.21: Vector sequences that minimize the number of switching transitions.

$\vec{v}_{\text{xdn}}, \vec{v}_{\text{xnd}}, \vec{v}_{\text{dnx}}, \vec{v}_{\text{ndx}}, \vec{v}_{\text{nxd}}, \vec{v}_{\text{dxn}}, \vec{v}_{\text{dxn}}, \vec{v}_{\text{nxd}}, \vec{v}_{\text{ndx}}, \vec{v}_{\text{dnx}}, \vec{v}_{\text{xnd}}, \vec{v}_{\text{xdn}}, \ldots$

also eliminates any switching transitions from $v_{\max}$ to $v_{\min}$. The maximum voltage switched never exceeds $\sqrt{3}V_{\text{in}}/\sqrt{2}$ where V_{in} the input voltage (line-to-line, rms). Since the switching losses are a function of the voltage switched, the above sequence is expected to reduce the switching losses further.

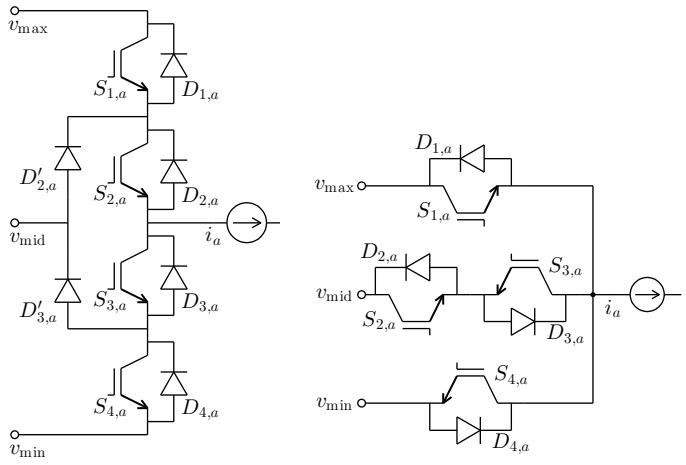
The above sequence also results in more symmetric number of transitions in the three output phases of any given load-side converter which is an important consideration for device packaging and thermal management.

Switching of the front-end converter

This section discusses the control of the front-end converter to generate the voltages $v_{\max}, \ldots$ Let,

$$
\begin{aligned}
s_{ab} &= \begin{cases} 1 & v_{ab} \geq 0 \\ 0 & v_{ab} < 0 \end{cases} \\
s_{bc} &= \begin{cases} 1 & v_{bc} \geq 0 \\ 0 & v_{bc} < 0 \end{cases} \\
s_{ca} &= \begin{cases} 1 & v_{ca} \geq 0 \\ 0 & v_{ca} < 0 \end{cases}
\end{aligned}
\tag{2.39}
$$

The signals s_{ab}, s_{bc}, s_{ca} are called the status signals corresponding to the input line-to-line voltages v_{ab}, v_{bc}, v_{ca} respectively. If at some given instant, $v_a = \max(v_a, v_b, v_c)$,



(a) I-type (b) T-type

Figure 2.22: Phase legs of the indirect matrix converter based open-end winding drives using (a) the I-type and (b) the T-type three-level inverter structures.

it follows that $s_{ab} = 1, s_{ca} = 0$ assuming $v_{ab} \neq 0, v_{ca} \neq 0$. Therefore the signal $s_{ab}\overline{s}_{ca}$ could be used to control the connection of the input phase a to the $v_{\max}$ terminal, where $\overline{s}$ denotes logical negation of s.

Fig. 2.22 shows the phase leg a of the front-end converter for both, I-type and T-type, topologies. The circuits are, of course, identical to the phase legs of the load-end converters shown in Fig. 2.18. The switching signal $q_{i,j}$ corresponding to a switch $S_{i,j}$ of the front-converter can be derived as (2.40), where $i \in \{1, 2, 3, 4\}$ and $j \in \{a, b, c\}$.

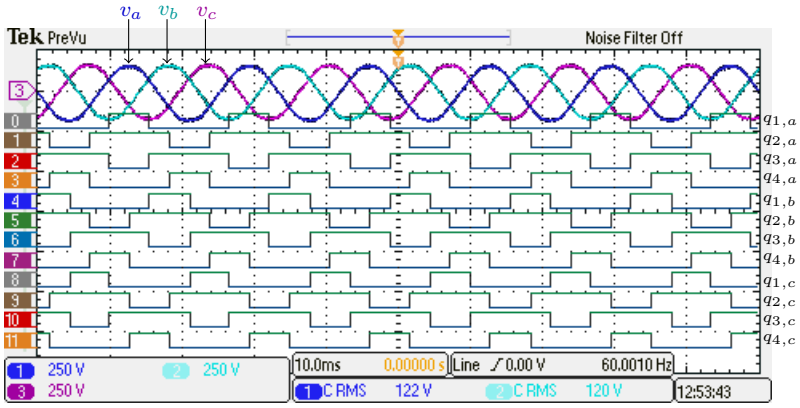


Figure 2.23: The switching signals for the front-end converter.

$$
\begin{aligned}
q_{1,a} &= s_{ab}\overline{s}_{ca} \quad (v_a = \max(v_a, v_b, v_c)) \\
q_{4,a} &= \overline{s}_{ab}s_{ca} \quad (v_a = \min(v_a, v_b, v_c)) \\
q_{2,a} &= \overline{q}_{4,a} \\
q_{3,a} &= \overline{q}_{1,a} \\
q_{1,b} &= s_{bc}\overline{s}_{ab} \quad (v_b = \max(v_a, v_b, v_c)) \\
q_{4,b} &= \overline{s}_{bc}s_{ab} \quad (v_b = \min(v_a, v_b, v_c)) \\
q_{2,b} &= \overline{q}_{4,a} \\
q_{3,b} &= \overline{q}_{1,a} \\
q_{1,c} &= s_{ca}\overline{s}_{bc} \quad (v_c = \max(v_a, v_b, v_c)) \\
q_{4,c} &= \overline{s}_{ca}s_{bc} \quad (v_c = \min(v_a, v_b, v_c)) \\
q_{2,c} &= \overline{q}_{4,a} \\
q_{3,c} &= \overline{q}_{1,a}
\end{aligned}
\tag{2.40}
$$

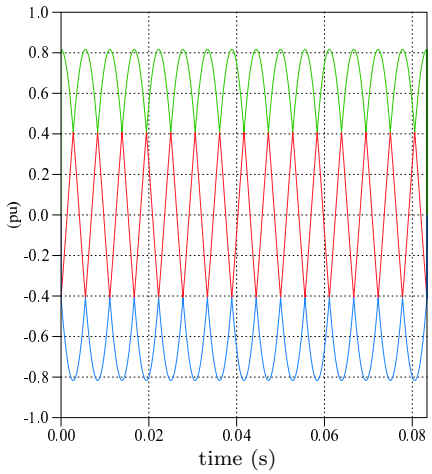
The signals $q_{i,j}$ for the front-end switches are shown in Fig. 2.23 for a 208 V, 60 Hz input voltage. It is seen that the switches of the front-end switch at 60 Hz. Furthermore, the switching transitions occur at the zero crossings of the line-to-line voltages resulting in zero voltage switching (ZVS). Therefore no switching losses occur in the front-end converter.

2.2.4 Simulation

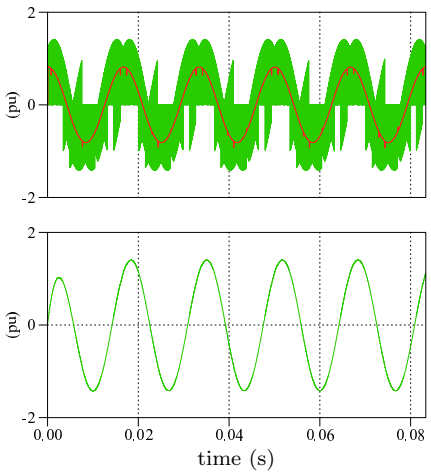
This section presents brief simulation results for the T-type indirect matrix converter based open-end winding drive. Identical results are obtained for the I-type topology as well. The conditions of the simulation are summarized in Table 2.6. The simulation results are shown in Fig. 2.24.

V_{base}	480 V	Voltage transfer ratio	1.0
S_{base}	80 kVA	Output frequency	60 Hz
Input	1.0 pu, 60 Hz	Load	Z_{base}, 0.8 (lagging)
Switching frequency	12 kHz	α	0.50
Carrier	Triangular	Grid current filter	None

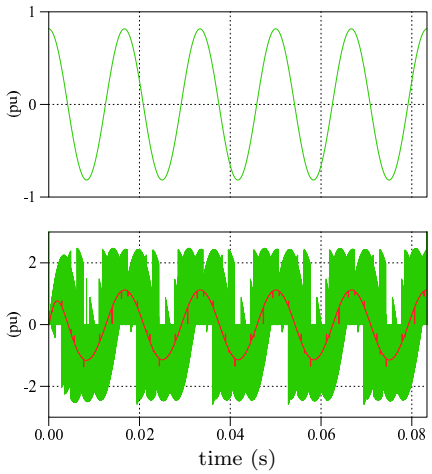
Table 2.6: Conditions of the simulation.



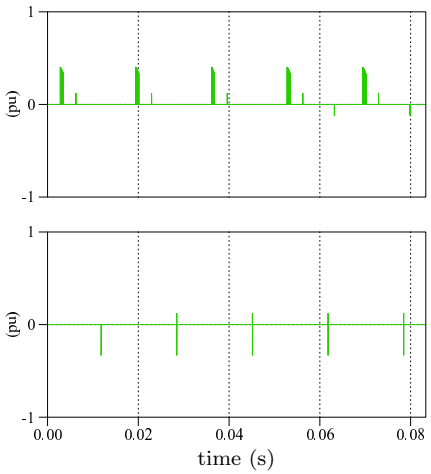
(a) Front-end output voltages $v_{\max}$, v_{mid}, and $v_{\min}$



(b) Load voltage $v_{A_1A_2}$ and its switching cycle average $\overline{v}_{A_1A_2}$ (top); output current i_A (bottom)



(c) Input voltage v_a (top); input current i_a and its switching cycle average $\overline{i}_a$ (bottom)



(d) Output common-mode voltages v_{CM_1} (top) and v_{CM_2} (bottom)

Figure 2.24: Simulation results for the T-type indirect matrix converter based open-end winding drive at the conditions of Table 2.6. The occasional glitches in the output common-mode voltage in (d) are one solution time step wide and are attributed to simulation inaccuracies.

2.3 Modulation of the direct matrix converter based open-end winding drive for common-mode elimination

The indirect matrix converter based open-end winding drives described in the previous sections generate a variable amplitude, variable frequency output by combinations of the positive and negative sequence link voltage vectors. The direct matrix converter based open-end winding drive generates its output by combinations of the positive and negative sequence input voltage vectors.

The link voltage vectors are equal in magnitude and speed to the input voltage vectors. Therefore the equation (2.14) and the vector diagram showing the output voltage synthesis (Fig. 2.15) are also applicable to the direct matrix converter based open-end winding drive with one minor change: $\{\vec{v}_1, \vec{v}_2, \vec{v}_3\}$ is either equal to $\{\vec{v}_{abc}, \vec{v}_{bca}, \vec{v}_{cab}\}$ or to $\{\vec{v}_{acb}, \vec{v}_{cba}, \vec{v}_{bac}\}$, instead of $\{\vec{v}_{\mathrm{xdn}}, \ldots\}$ or $\{\vec{v}_{\mathrm{xnd}}, \ldots\}$.

For the general case, in which both sets of vectors would be used for power factor control, equation (2.25)–(2.31) can be rewritten for the direct matrix converter based open-end winding drive as:

$$\mathbf{V}_{\mathrm{pos}} = [\vec{v}_{abc}\, \vec{v}_{bca}\, \vec{v}_{cab}]^T \tag{2.41}$$

$$\mathbf{V}_{\mathrm{neg}} = [\vec{v}_{acb}\, \vec{v}_{cba}\, \vec{v}_{bac}]^T \tag{2.42}$$

$$\mathbf{\Lambda}_{1,\mathrm{pos}} = [\lambda_{1,abc}\, \lambda_{1,bca}\, \lambda_{1,cab}] \tag{2.43}$$

$$\mathbf{\Lambda}_{1,\mathrm{neg}} = [\lambda_{1,acb}\, \lambda_{1,cba}\, \lambda_{1,bac}] \tag{2.44}$$

$$\mathbf{\Lambda}_{2,\mathrm{pos}} = [\lambda_{2,abc}\, \lambda_{2,bca}\, \lambda_{2,cab}] \tag{2.45}$$

$$\mathbf{\Lambda}_{2,\mathrm{neg}} = [\lambda_{2,acb}\, \lambda_{2,cba}\, \lambda_{2,bac}] \tag{2.46}$$

$$\vec{v}^* = \alpha(\mathbf{\Lambda}_{1,\mathrm{pos}} - \mathbf{\Lambda}_{2,\mathrm{pos}})\mathbf{V}_{\mathrm{pos}} + (1-\alpha)(\mathbf{\Lambda}_{1,\mathrm{neg}} - \mathbf{\Lambda}_{2,\mathrm{neg}})\mathbf{V}_{\mathrm{neg}} \tag{2.47}$$

Since the balanced input voltages add to zero, the output voltages at both motor terminals also add to zero resulting in zero common-mode voltage. To achieve intelligent commutation in the direct matrix converter based open-end winding drive, accurate knowledge of the current direction is necessary. Clamp circuits are required to avoid unintended interruptions of the load currents.

Loss-optimal vector sequences can be derived for this drive as well, same as the indirect matrix converter based open-end winding drive. Either of the two sequences

A_1	B_1	C_1	A_1	B_1	C_1
a	b	c	a	b	c
a	c	b	a	c	b
b	c	a	b	c	a
c	b	a	b	a	c
c	a	b	c	a	b
b	a	c	c	b	a
b	a	c	c	b	a
c	a	b	c	a	b
c	b	a	b	a	c
b	c	a	b	c	a
a	c	b	a	c	b
a	b	c	a	b	c
20 transitions			20 transitions		

Table 2.7: Loss-optimal switching sequences for the DMC OE Wdg. drive.

in Table 2.7 can be used. It was seen in the indirect drive (Table 2.5, Fig. 2.21) that one sequence eliminated the $v_{\max} \leftrightarrow v_{\min}$ switching transitions. This feature cannot be realized in the direct matrix converter based drive and all switches will switch the peak line-to-line voltage at some point during the drive operation.

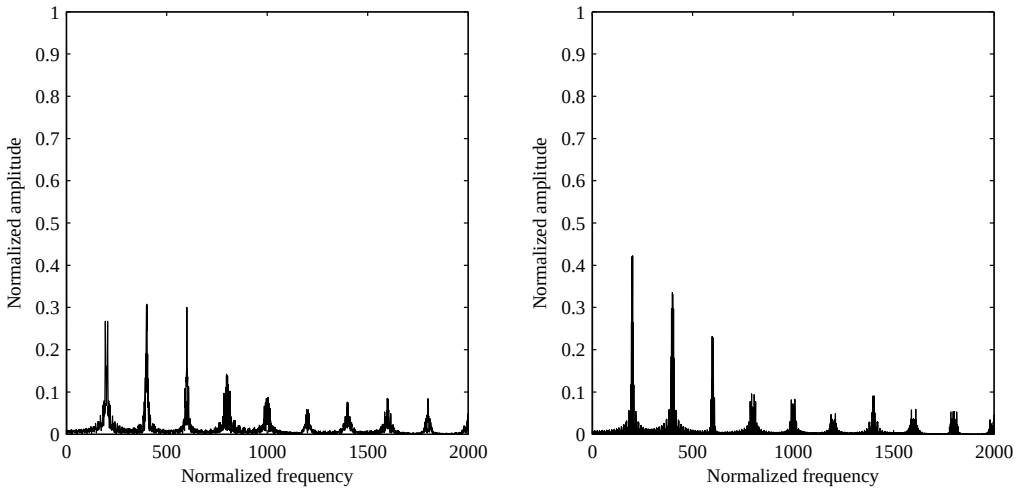
2.4 Input filter

Fig. 2.25 shows the spectra of the simulated input current for the conditions of Table 2.6. Results for the T-type indirect matrix converter based open-end winding drive are shown in Fig. 2.25(a) and Fig. 2.25(b) shows the results for the direct matrix converter based open-end winding drive.

It is seen that both converters have significant harmonic content centered at the multiples of the switching frequency. In a per-phase equivalent circuit, the unfiltered input current can be expressed as:

$$i_{\text{sw}} = i_1 + \tilde{i}_{\text{sw}} \tag{2.48}$$

Where i_{sw} is the unfiltered current generated by the PWM matrix converter, i_1 is the fundamental input current and $\tilde{i}_{\text{sw}}$ represents the harmonic current at and around the multiples of the switching frequency. This harmonic current is also called ripple



(a) T-type (b) DMC

Figure 2.25: Simulated spectra of the unfiltered input currents.

current since it appears as a zero-mean current 'riding' on the desired fundamental current. Assuming that $f_1 \ll f_{\text{sw}}$, $i_1 = \bar{i}_{\text{sw}}$ where the bar denotes the the switching cycle average, where f_1 is the input fundamental frequency (fundamental) and f_{sw} is the switching frequency.

For compliance with various international standards, it is necessary that the grid current be sinusoidal. Therefore a filter is necessary to avoid injecting $\tilde{i}_{\text{sw}}$ into the grid. Intuitively, a filter must:

- Impede the flow of the harmonic current into the grid, and
- provide an alternative low-impedance path to the harmonic current.

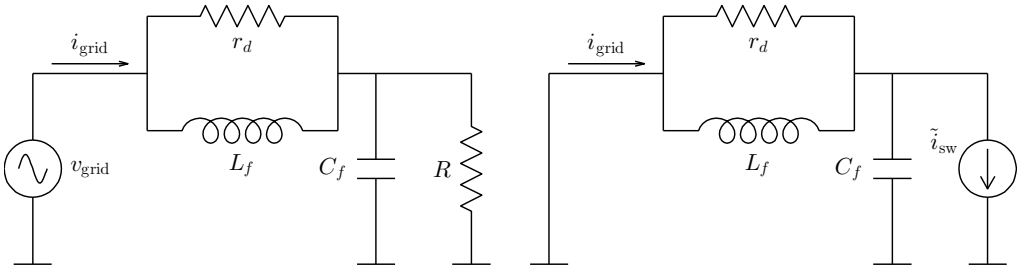
2.4.1 A second-order LC filter

Since the ripple current is comprised of high-frequency components, an inductor in series with the input voltage source impedes its flow into the grid; a capacitor connected across the source of the harmonic current can be used to shunt the harmonic current away from the grid. Combined, the inductor and the capacitor form a second order LC filter that filters the input current such that the grid current is sinusoidal.

An undamped LC filter is impractical for matrix converter applications since the amplification at the resonant frequency is limited only by the parasitic resistances; if excited by a frequency sufficiently close to the resonant frequency, destructive currents and voltages will appear in the system. Therefore a damping resistor r_d is used. Multiple locations for the damping resistor are possible that have been analyzed in [74, 75]. Generally, a damping resistor connected in parallel with the input inductor is used and will be treated as the reference filter topology in this section. Fig. 2.26 shows the single-phase equivalent circuit of this reference filter topology at the fundamental frequency and the harmonic frequencies. The converter and the driven load are represented by an equivalent resistance R at the fundamental frequency. The filter components are L_f, C_f and a damping resistor r_d. Let,

$$\begin{aligned} \omega_0 &= \frac{1}{\sqrt{L_f C_f}} \\ \zeta &= \frac{1}{2r_d}\sqrt{\frac{L_f}{C_f}} \end{aligned} \tag{2.49}$$

The transfer functions corresponding to the equivalent circuits in Fig. 2.26 can now



(a) Filter circuit at the fundamental frequency (b) Filter circuit at the harmonic frequencies

Figure 2.26: Filter circuit at the (a) fundamental and the (b) harmonic frequencies.

be defined as:

$$\frac{i_{\text{grid}}(s)}{\tilde{i}_{\text{sw}}(s)} = \frac{2\zeta\omega_0 s + \omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \tag{2.50}$$

$$\frac{i_{\text{grid}}(s)}{v_{\text{grid}}(s)} = \frac{1}{r_d}\left(\frac{s^2 + s\left(\frac{r_d}{L_f} + \frac{1}{RC_f}\right) + \omega_0^2\frac{r_d}{R}}{s^2 + \frac{s}{C}\left(\frac{r_d + R}{r_d R}\right) + \omega_0^2}\right) \tag{2.51}$$

For the input filter to be effective:

- The filter must attenuate the current ripple, i.e. $|i_{\text{grid}}(j\omega)/\tilde{i}_{\text{sw}}(j\omega)|_{\omega \gtrapprox 2\pi f_{\text{sw}}} \approx 0 : i_{\text{grid}} \approx i_{1,\text{grid}}$
- The damping resistor must limit the amplification at the damped resonant frequency, i.e. $\|i_{\text{grid}}/\tilde{i}_{\text{sw}}\|_\infty \sim 1$
- The fundamental power dissipation in the damping resistor must be low, i.e. $i_{1,r_d} \ll i_{1,\text{grid}}$
- The fundamental current drawn by the filter capacitor must be small, i.e. $i_{1,C_f} \approx 0 : i_{1,\text{grid}} \approx i_1$

The transfer function $i_{\text{grid}}/\tilde{i}_{\text{sw}}$ (2.50) is plotted in Fig. 2.27 for two values of the damping coefficient ζ. Let $\omega_1 := 2\pi f_1$. Some L_f, C_f were chosen such that $\omega_0 = 10\,\omega_1$, and ζ was controlled using r_d. Following conclusions can be drawn based on Fig. 2.27 and the preceding discussion:

- Even though two poles are present in the transfer function (2.50), the presence of a zero degrades the attenuation to $-20\,\text{dB/decade}$. This zero is an unavoidable consequence of a finite damping ratio ζ.
- Amplification at the damped resonant frequency falls with ζ. However, for fixed L_f, C_f, a higher ζ means a higher L_f/r_d ratio, which has the adverse effect of increased power losses in r_d since a higher fraction of the fundamental current now flows through the damping branch.

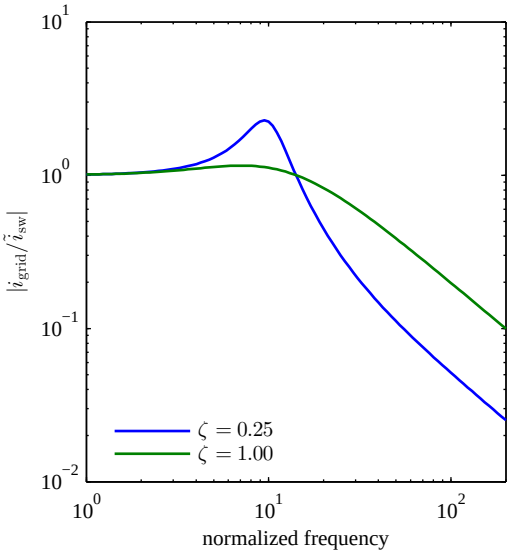


Figure 2.27: $i_{\text{grid}}/\tilde{i}_{\text{sw}}$ for a second-order filter.

For an acceptable damping ratio ζ, increasing L_f, C_f while keeping the ratio L_f/C_f fixed ($\because \zeta \propto \sqrt{L_f/C_f}$), has the effect of shifting the frequency response to the left, leading to better absolute attenuation in the high-frequency range. However, increasing L_f, C_f implies:

- larger values of the reactive components,
- larger fundamental current i_{1,C_f} drawn by the capacitor C_f, and
- a higher L_f/r_d ratio leading to additional power dissipation.

2.4.2 A third-order filter

Based on the discussion in the previous section, a second-order filter may fail to attenuate the harmonics effectively while maintaining acceptable damping, low fundamental filter current i_{1,C_f}, and low values of the reactive components. Higher-order filters can provide better attenuation than a second-order filter at a lower cost and have been investigated for DC-DC converters [76], AC-DC grid-tied inverters [12, 77], and matrix converters [75, 78].

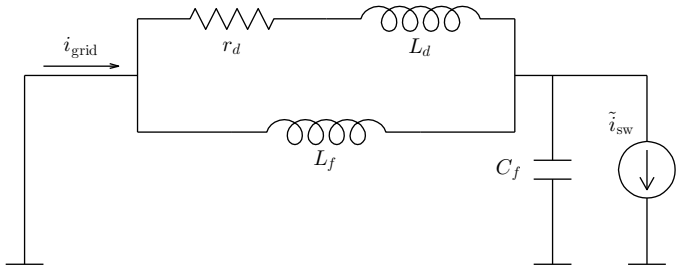


Figure 2.28: A third-order input filter.

Among other topologies, a filter with the damping resistor of Fig. 2.26 replaced by a series RL branch was proposed in [76]. This filter is shown in Fig. 2.28 for the present case. The resistor r_d in the damping branch provides the necessary damping. At higher frequencies, the impedance of the series RL branch is dominated by the inductance L_d — therefore, the flow of the ripple current into the input is impeded by the parallel combination of the input inductor L_f and the damping branch inductor L_d.

Reference [76] optimized the value of r_d for a given L_d/L_f such that the peak output impedance of the filter is minimized. In this section, r_d is optimized to minimize $\|i_{\text{grid}}/\tilde{i}_{\text{sw}}\|_\infty$ for a given L_d/L_f. The motivation for this choice lies in the spectra of the unfiltered current i_{sw} in Fig. 2.25: the spectra are plotted for a switching frequency $f_{\text{sw}} = 200\, f_1$. The harmonic components are centered at the multiples of the switching frequency. It is possible, especially at lower switching frequencies, that some harmonic components lie close to the damped natural frequency. To ensure that no components at $\omega < 2\pi f_{\text{sw}}$ are amplified, it is necessary to find an r_d that minimizes $\|i_{\text{grid}}/\tilde{i}_{\text{sw}}\|_\infty$. In this section:

- $\|i_{\text{grid}}/\tilde{i}_{\text{sw}}\|_\infty$ is minimized for a given choice of L_d/L_f, and
- r_d is calculated such that $\|i_{\text{grid}}/\tilde{i}_{\text{sw}}\|_\infty$ is equal to its minima.

Let,

$$n := L_d/L_f \tag{2.52}$$

$$\begin{aligned} G(s) &:= \frac{i_{\text{grid}}(s)}{\tilde{i}_{\text{sw}}(s)} \\ &= \frac{sL_f(n+1) + r_d}{s^3 n L_f^2 C_f + s^2 L_f C_f r_d + sL_f(n+1) + r_d} \end{aligned} \tag{2.53}$$

The transfer function $G(s)$ has three poles and one zero as opposed to two poles and one zero in the corresponding transfer function for the second-order system. Therefore the high-frequency attenuation provided by $G(s)$ is $-40\,\mathrm{dB/decade}$. This is shown in Fig. 2.29 for some values of L_f, C_f common to both filters, second-order and third-order, and some values of the damping branch component(s).

It is easy to see in Fig. 2.28 that the third-order filter reduces to an undamped second order filter for $r_d = \infty$ (L_f, C_f) and for $r_d = 0$ $(L_f \| L_d, C_f)$. The transfer function $G(s)$ is plotted for a few different values of r_d for some n in Fig. 2.30. It is observed that for a given $n, \exists \omega^* : G(j\omega^*)$ is independent of r_d $\forall r_d \geq 0$. Therefore it is possible to find r_d that will minimize $\|G(j\omega)\|_\infty$: the infinity-norm of G is the maximum amplification the filter can across all frequencies, and it is desirable that the amplification be as low as possible, approaching unity only at the fundamental frequency. This frequency can be calculated by equating $|G(j\omega)|_{r_d=0}$ and $|G(j\omega)|_{r_d=\infty}$, and is found as:

$$\omega^* = \sqrt{\frac{2(n+1)}{2n+1}}\,\omega_0 \tag{2.54}$$

$$|G(j\omega^*)| = 2n+1 \qquad \forall\, r_d \geq 0 \tag{2.55}$$

Let $k := L_f/r_d$, $f(k, j\omega) := |G(k, j\omega)|^2$. To find the optimal value of r_d, it sufficient

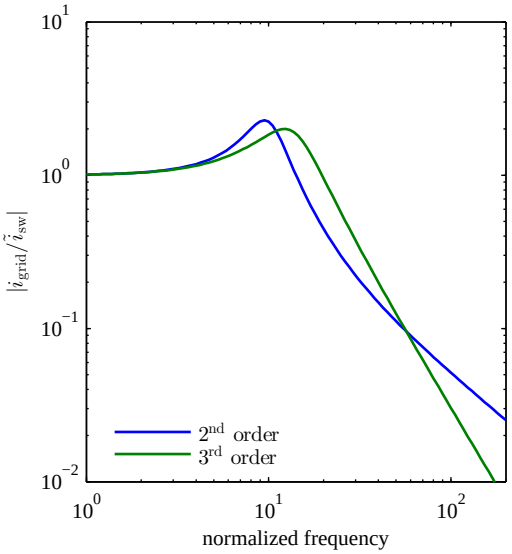


Figure 2.29: $i_{\mathrm{grid}}/\tilde{i}_{\mathrm{sw}}$ for a second-order and a third-order input filter.

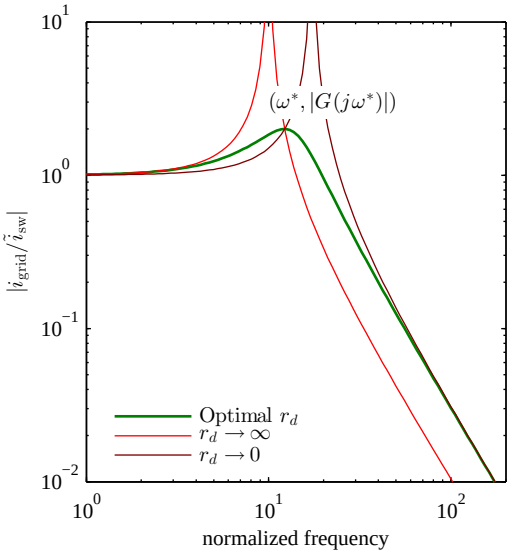


Figure 2.30: $G(s)$ for some n at different r_d.

to find $k : \|f(k, j\omega)\|_\infty = f(k, j\omega^*)$. In other words, the optimal value of k would be one for which the absolute value of the transfer function G is maximized at ω^*: since $|G(j\omega)| > 0\ \forall\omega$, the maxima of $|G|$ and $f = |G|^2$ occur at the same value of ω.

$$f(k, j\omega) = \frac{1 + k^2\omega^2(n+1)^2}{(1 - \omega^2/\omega_0^2)^2 + k^2\omega^2(n + 1 - n\omega^2/\omega_0^2)^2} \tag{2.56}$$

$$\begin{aligned} f'(k, j\omega)\big|_{\omega=\omega^*} \propto\ & 2k^2\omega^*(n+1)^2 \left[\left(1 - \frac{\omega^{*2}}{\omega_0^2}\right)^2 + k^2\omega^{*2}\left(n + 1 - n\frac{\omega^{*2}}{\omega_0^2}\right)^2\right] \\ & - \left(1 + k^2\omega^{*2}(n+1)^2\right)\left[2\left(1 - \frac{\omega^{*2}}{\omega_0^2}\right)\left(-2\frac{\omega^*}{\omega_0^2}\right)\right. \\ & \qquad + 2k^2\omega^*\left(n + 1 - n\frac{\omega^{*2}}{\omega_0^2}\right)^2 \\ & \qquad \left. + 2k^2\omega^{2*}\left(n + 1 - n\frac{\omega^{*2}}{\omega_0^2}\right)\left(-2n\frac{\omega^*}{\omega_0^2}\right)\right] \end{aligned} \tag{2.57}$$

The above expression doesn't include the square of the denominator of the expression being differentiated. Upon maximizing, the optimal value of k is obtained as:

$$k = \frac{1}{\omega_0}\sqrt{\frac{n + \frac{1}{2}}{n(n+1)^2}} \tag{2.58}$$

Design of a third-order filter

To design a third-order filter, we will start with a second-order filter. It is first necessary to define the per-unit system used. The design would be in per-unit for easy adaptation to different systems. For a given system $V_{\text{base}}, S_{\text{base}}, f_{\text{base}}$, the base quantities are defined in (2.59).

$$\begin{aligned} I_{\text{base}} &= \frac{1}{\sqrt{3}} \frac{S_{\text{base}}}{V_{\text{base}}} \\ Z_{\text{base}} &= \frac{V_{\text{base}}^2}{S_{\text{base}}} \\ \omega_{\text{base}} &= 2\pi f_{\text{base}} \\ L_{\text{base}} &= \frac{Z_{\text{base}}}{\omega_{\text{base}}} \\ C_{\text{base}} &= \frac{1}{\omega_{\text{base}} Z_{\text{base}}} \end{aligned} \tag{2.59}$$

Let the switching frequency f_{sw} be $\geq 100\, f_1$. The filter design is shown in the steps below. It should be stressed that the design may not progress linearly, and it may be necessary to repeat certain steps based on simulation results with the converter and availability of the components.

1. Choose the natural frequency ω_0 to be $10\,\omega_1$ such that the damped resonant frequency is sufficiently higher than the fundamental and sufficiently lower than the switching frequency.

2. 3%–5% input reactors are commonly available off-the-shelf for AC drives applications. Cost and design-time savings can be realized by choosing an off-the-shelf input reactor for the inductor L_f. A 3% inductance is initially chosen.

3. The choice of the natural frequency and the inductance fixes the value of the capacitance.

4. The damping coefficient ζ is chosen to be 0.25 and the value of r_d is calculated from (2.49).

At this stage the second-order filter is designed. The frequency response of this filter

is shown in Fig. 2.27 and again in Fig. 2.29. The performance of this filter in the single-phase equivalent circuit of Fig. 2.26(a) with $v_{\text{grid}} = 1\,\text{pu}$ and $R = Z_{\text{base}}$ is summarized in Table 2.8. The performance was also found to be satisfactory in the power electronic simulation.

Loss at full-load	0.17%
Full-load power factor	95.79%

Table 2.8: Performance of the second-order filter at the fundamental frequency.

By increasing L_f while holding ω_0 constant, the full-load power factor can be improved at the cost of increased losses in the damping resistor. By increasing both, L_f and C_f, while holding ζ constant, the absolute high-frequency attenuation can be improved at the cost of increased losses and poorer full-load power factor.

To extend the design to a third-order filter, it is necessary to pick a value of n ($= L_d/L_f$) and then calculate r_d from (2.58). Fig. 2.31 shows the frequency response of the third-order filter for different values of n. As expected from (2.54), the maximum amplification falls with n. However, reducing n also means higher current rating of the damping branch components r_d, L_d and increased losses. This is summarized in

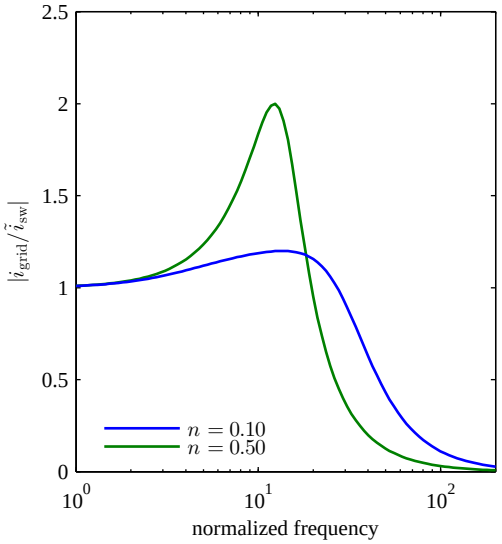


Figure 2.31: Dependence of $\|G\|_\infty$ on n.

	$n = 0.10$	$n = 0.50$
Current carried	22.86%	9.91%
Power loss	0.70%	0.31%

Table 2.9: Current rating and damping losses as a function of n at rated load.

Table 2.9. The response of the third-order filter with $n = 0.5$ is compared against the second-order filter designed earlier in Fig. 2.32. Both filters use the same L_f, C_f. The damping resistor in the second-order filter is determined by $\zeta = 0.25$ whereas the damping inductor and resistor for the third-order filter are chosen using $n = 0.5$ and (2.58).

The third-order filter provides better absolute attenuation at $\omega \gtrapprox 70\,\omega_1$. Even though an additional inductor is used, it carries only a tenth of the fundamental current and would therefore be insignificant in size and cost compared to the main inductor. For switching frequencies $f_{\text{sw}} \approx 100\,f_1$, this third-order filter is acceptable. Losses in the damping branch can be reduced further by increasing the value of n.

If the switching frequency is higher, then the $-40\,\text{dB/decade}$ attenuation can be used to shrink the components of the third-order filter (in the designs of Fig. 2.32, both

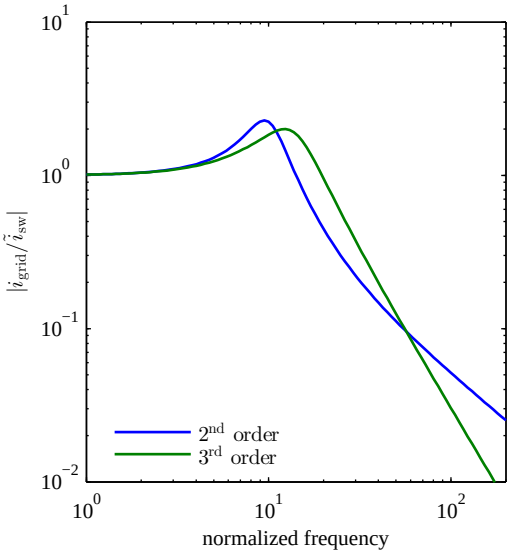


Figure 2.32: $i_{\text{grid}}/\tilde{i}_{\text{sw}}$ for a second-order and a third-order input filter.

filters use the same L_f, C_f). Let us, somewhat arbitrarily, reduce the inductance L_f to two-thirds of its value and the capacitance to half. Let n be changed to 1/3. L_d, r_d can be determined now. Fig. 2.33 shows the frequency response of this filter along with the second-order filter designed earlier. This filter $2L_f/3, C_f/2, n = 1/3$ is tuned to arrive at the design titled third-order final design in Fig. 2.33 that has the same attenuation as the second-order design at $\omega = 200\,\omega_1$. The tuning is based on performance in power electronic simulations as well as the availability of the components. The two filters, second-order and third-order final design, are compared in Table 2.10.

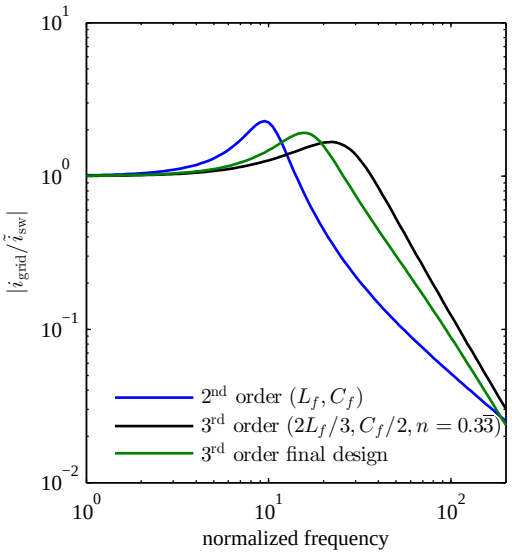


Figure 2.33: $i_{\text{grid}}/\tilde{i}_{\text{sw}}$ for the designed second-order and third-order input filters.

	Second-order	Third-order
L_f	0.0300	0.0261
C_f	0.3333	0.1631
L_d	–	0.0083
r_d	0.6000	0.5547
Power loss in the damping branch	0.0017	0.0013
Current carried by the damping branch	0.0531	0.0477
Power factor	0.9579	0.9909

Table 2.10: A comparison of the designed second-order and third-order input filters. The power loss and current rating of the damping branch, and the power factor are specified at full-load.

Fig. 2.33 and Table 2.10 clearly show the superiority of the third-order filter over its second-order counterpart. Even though the designs are somewhat partial to higher switching frequencies ($f_{\text{sw}} \gtrapprox 200\, f_1$, Fig. 2.25), a third-order filter more compact than a second-order filter can always be designed. In the remainder of this dissertation, the third-order design of Table 2.10 will be used for the presented drives unless mentioned otherwise. Fig. 2.34 and Table 2.11 show the frequency response and component values for the prototypes of the filters of Table 2.10 for a 208 V, 3 kVA system. The values of Table 2.11 have been used in the prototypes presented in the next section.

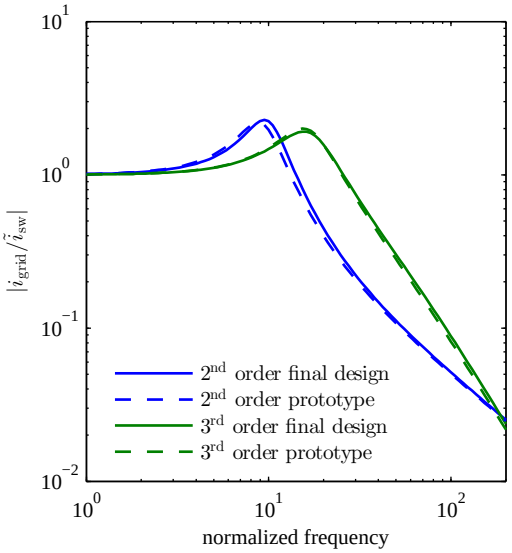


Figure 2.34: $i_{\text{grid}}/\tilde{i}_{\text{sw}}$ for the filters: designs and prototypes.

	Second-order	Third-order
L_f	1.5 mH	0.95 mH
C_f	18 μF(Δ)	10.75 μF(Δ)
L_d	–	330 μH
r_d	10 Ω	8 Ω

Table 2.11: Components used in the prototypes.

2.5 Experimental results

This section shows the experimental results from the prototypes of the two indirect matrix converter based open-end winding drives. Evidence of the high voltage transfer ratio and input power factor control is provided. Current sensor-less intelligent commutation and clamp circuit-less operation is demonstrated. These results establish the functionality of the indirect matrix converter based drives on par with their direct counterpart, and also prove the additional advantages unique to the indirect implementations.

The filters designed in Table 2.11 are used and similar attenuation of the switching frequency harmonics is observed with the larger second-order filter and the more compact third-order filter validating the approach proposed. Sources of distortion in the input/output currents in spite of adequate filtering are identified.

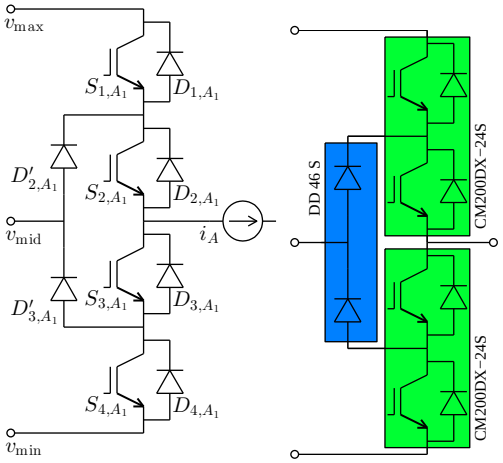
Discussion of the common-mode voltage elimination is reserved for a later chapter.

2.5.1 Prototypes of the indirect matrix converter based drives

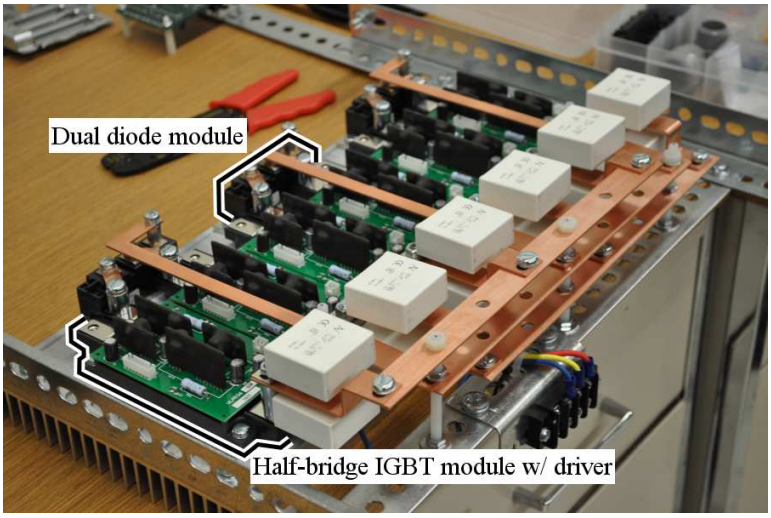
I-type

A prototype of the I-type indirect matrix converter drive was constructed using the CM200DX-24S half-bridge IGBT module by Powerex, Inc. and DD 46 S dual diode module by Infineon Technologies AG. Two half-bridge modules and one dual diode module form one phase leg as illustrated in Fig. 2.35(a). Three such legs from one converter which can be employed as the front-end converter or either of the two load-end converters. One such converter is pictured in Fig. 2.35(b). A photograph of the entire drive comprised of the three converters and the input filter is shown in Fig. 2.38(a). The IGBTs are driven using VLA536-01R gate driver board by Powerex, Inc.

The I-type drive prototype uses the second-order filter of Table 2.11.



(a) Modules used



(b) Photograph of one converter

Figure 2.35: Construction of the I-type indirect matrix converter based open-end winding drive. Three converters of (b) form the full circuit shown in Fig. 2.38(a).

T-type

The T-type indirect matrix converter drive was constructed using the T-type three-level inverter module APTGLQ40HR120CT3G by Microsemi Corporation. Nine such modules were used to construct the three identical converters as illustrated in Fig. 2.36. All three legs of all three converters are connected at a common $v_{\max}, v_{\text{mid}}, v_{\min}$ three-level bus. The busbar is a printed circuit board with pads for assembling the filter capacitors. The gate drivers were designed using the ACPL332J gate driver IC from Avago Technologies. The T-type drive prototype uses the third-order filter of Table 2.11.

A side-by-side drawing of the three-phase inductor used for L_f and the three individual inductors used for L_d is shown in Fig. 2.37. It is seen that the even though L_d has approximately third the inductance as L_f, the physical size is much smaller because of its lower current rating.

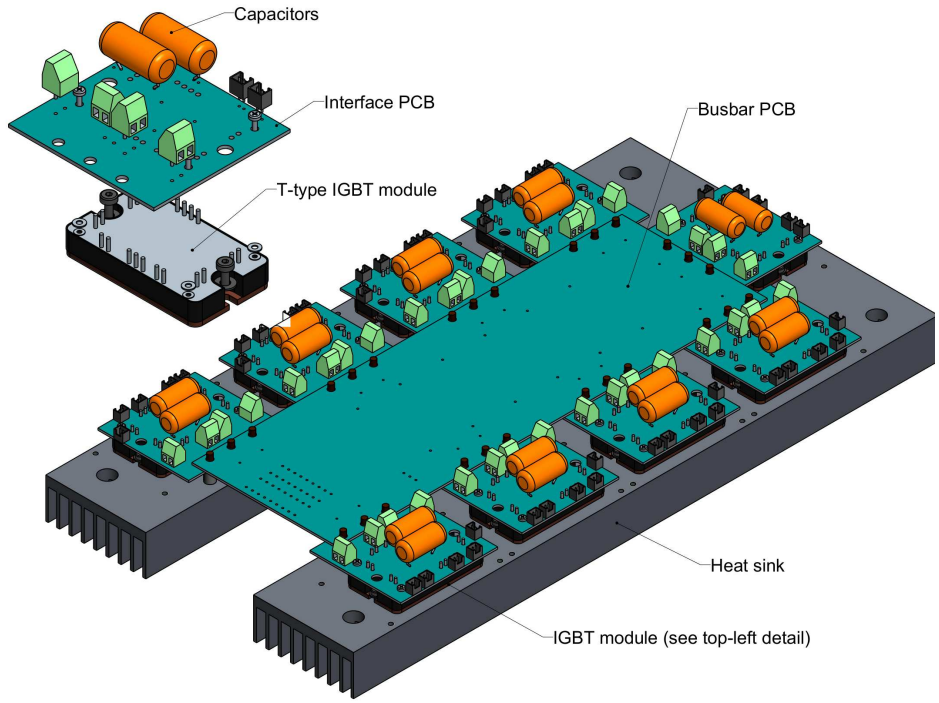


Figure 2.36: Construction of the T-type indirect matrix converter based open-end winding drive.

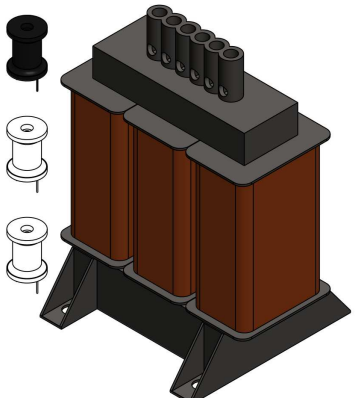
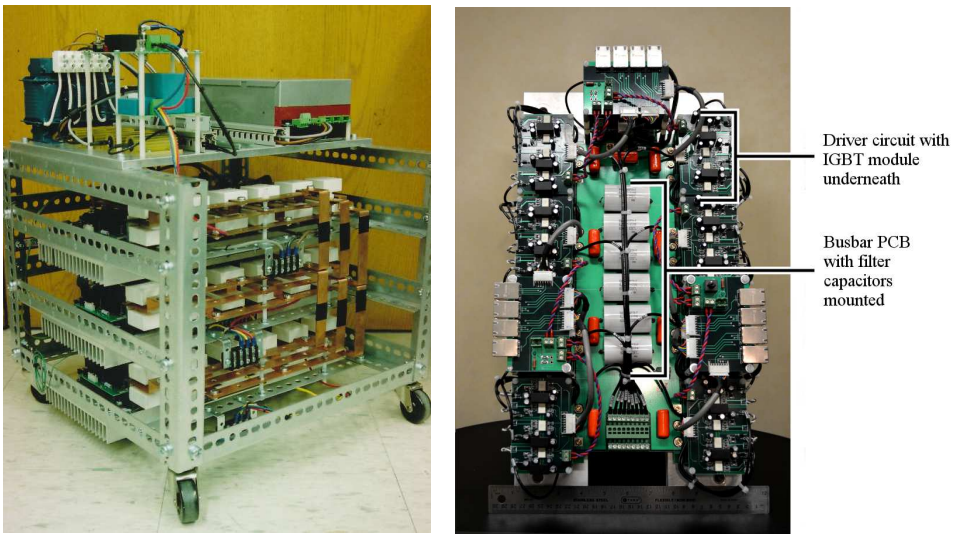


Figure 2.37: A comparison of the sizes of L_f and L_d for the third-order filter in Table 2.11. Scale = 1:3. L_f is 0.95 mH, three-phase rated for 10.7 A; L_d is 330 μH rated for 1.72 A.

A photograph of the drive excluding the filter inductor L_f and the damping components L_d, r_d is shown in Fig. 2.38(b).



(a) I-type (b) T-type

Figure 2.38: Photographs of the prototypes of the indirect matrix converter based open-end winding drives.

2.5.2 Experimental results

Experimental setup

The experimental setup uses the prototypes described in the previous section and the filters of Table 2.11. The input to the setup is a 208 Volts, 60 Hz three-phase outlet stepped down using a variac. The load is either a three-phase AC induction motor modified into an open-end winding machine, or a three-phase RL load.

The setup is described in Table 2.12. Details of the loads used are supplied in Table 2.13.

The input voltage is stepped down from 208 Volts to approximately 135 Volts such that the load voltage doesn't exceed 200 Volts at higher voltage transfer ratios. The load voltage is controlled in open-loop according to $V/f = 200/60$ and the desired output frequency, with the V/f constant based on the motor nameplate values. Same voltage control law is used for the RL load for consistency.

A separately excited DC machine, Baldor CD6203, acts as the mechanical load.

Results

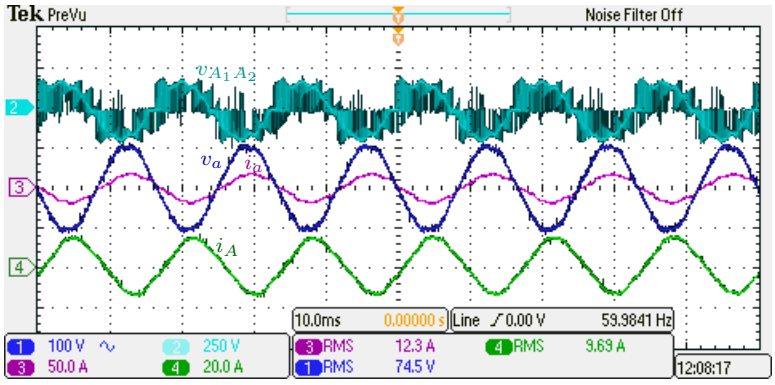
Fig. 2.39 shows the experimental input and output voltages and currents for the two topologies, I-type and T-type. The input voltage in both cases is approximately 135 Volts (line-to-line, rms), the switching frequency is approximately 10 kHz. The spectra of the

Topology	Input filter	Load
I-type	Second-order (Table 2.11)	ACIM (Table 2.13)
T-type	Third-order (Table 2.11)	Passive RL (Table 2.13)

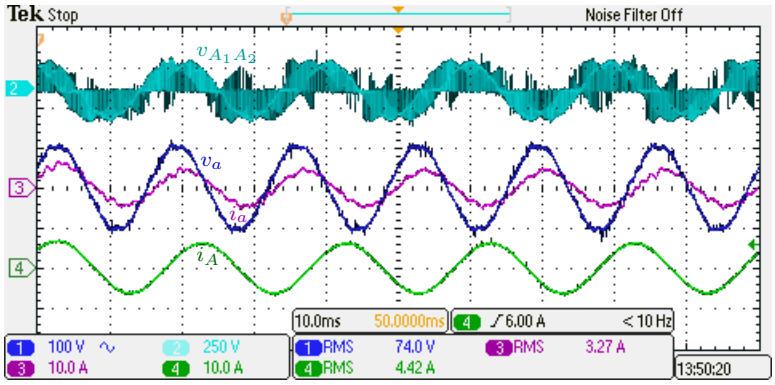
Table 2.12: Experimental setup.

ACIM	Make	Baldor	CAT.NO.	M3611T-8
	HP	3	RPM	1745
	VOLTS	200	HZ	60
	AMP	9.5	PF	78
RL	$10\,\Omega, 45$ mH nominal			

Table 2.13: Loads used.



(a) Inputs v_a, i_a and outputs $v_{A_1A_2}, i_A$ for the I-type topology. Input voltage $V_{ab} \approx 135\,\text{V}$; power factor control parameter $\alpha = 0.60$; output fundamental frequency $f_{\text{out}} = 60\,\text{Hz}$.

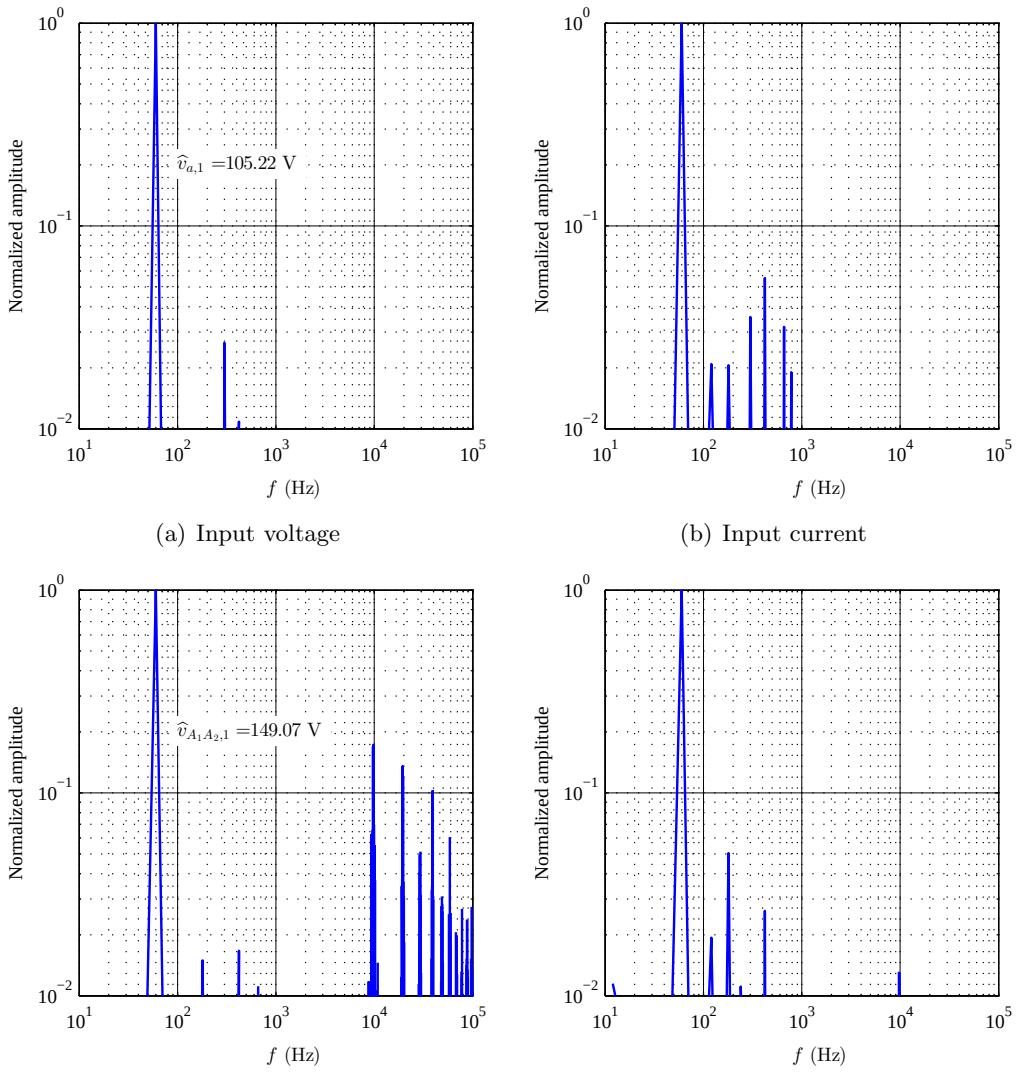


(b) Inputs v_a, i_a and outputs $v_{A_1A_2}, i_A$ for the I-type topology. Input voltage $V_{ab} \approx 135\,\text{V}$; power factor control parameter $\alpha = 0.70$; output fundamental frequency $f_{\text{out}} = 50\,\text{Hz}$; switching frequency $f_{\text{sw}} \approx 10\,\text{kHz}$.

Figure 2.39: Input and output waveforms for the two indirect matrix converter based open-end winding drives: (a) I-type and (b) T-type.

waveforms in these figures are shown in Fig. 2.40 (I-type) and Fig. 2.41 (T-type). Following observations are made from Figs. 2.39 – 2.41:

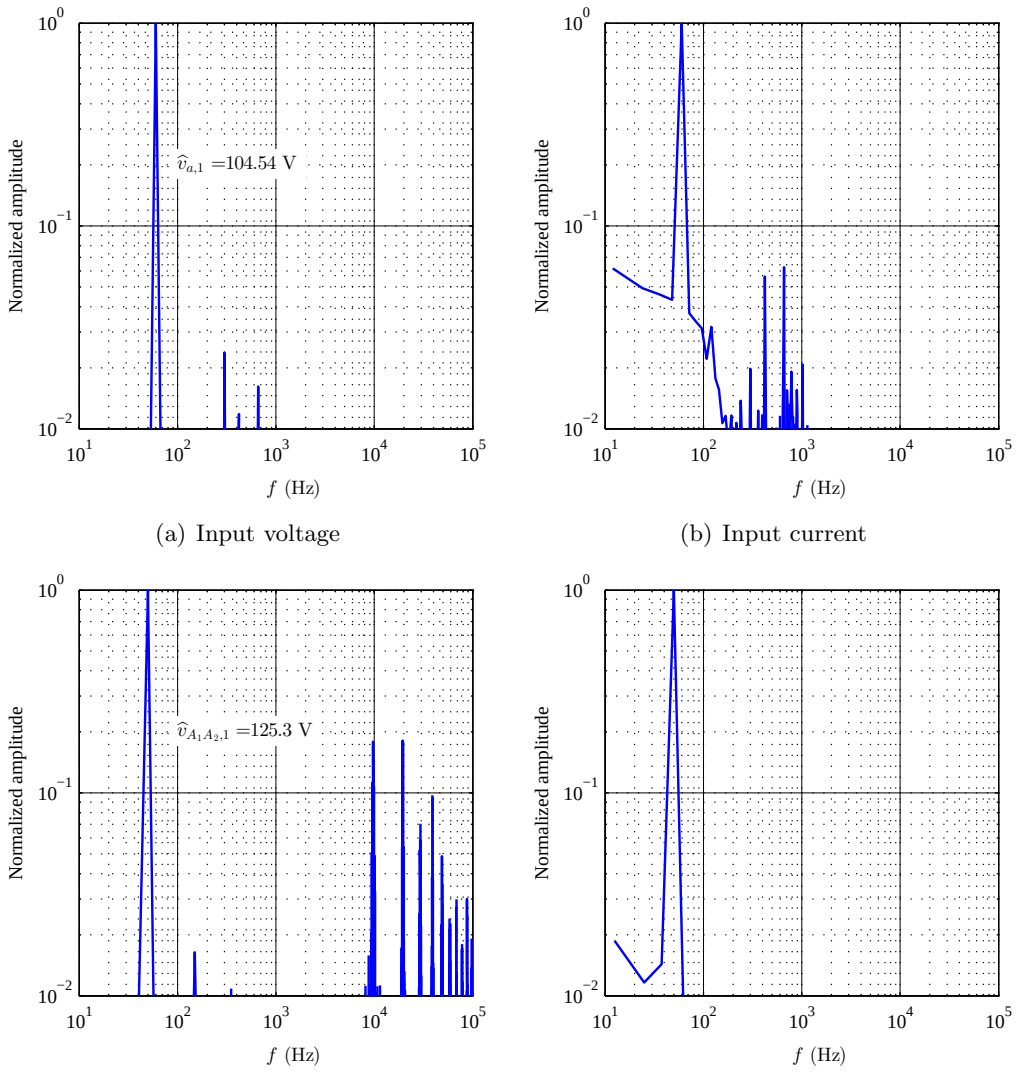
- The output voltage has a fundamental component and harmonics centered at the multiples of the switching frequency.
- The voltage transfer ratio ($\widehat{v}_{A_1A_2,1}/\widehat{v}_{a,1}$) in Fig. 2.40 is 1.42, and the voltage transfer ratio in Fig. 2.41 is 1.20 – these prove that the indirect matrix converter based open-end winding drives can generate voltages higher than the input voltage.



(a) Input voltage (b) Input current

(c) Output voltage (d) Output current

Figure 2.40: Spectra of the input and the output quantities for the I-type indirect matrix converter based open-end winding drive. Input frequency = 60 Hz, output frequency = 60 Hz, switching frequency ≈ 10 kHz.



(a) Input voltage (b) Input current

(c) Output voltage (d) Output current

Figure 2.41: Spectra of the input and the output quantities for the T-type indirect matrix converter based open-end winding drive. Input frequency = 60 Hz, output frequency = 50 Hz, switching frequency ≈ 10 kHz.

- According to the V/f control law, the output voltage in Fig. 2.40(c) must be 200 Volts and the output voltage in Fig. 2.41(c) must be 166.67 Volts. However, the output voltages in Fig. 2.40(c) and 2.41(c) are 182.57 Volts and 153.46 Volts respectively (output voltage means the effective line-to-line rms voltage). This discrepancy is attributed to:
  - Loading of the input transformer, and
  - reduced voltage transfer ratio due to device voltage drops.

  Both of the above phenomena, loading and device drops, occur at finite currents. Therefore the experiments were repeated with the load terminals open-circuited. Results in Fig. 2.42 show that the drive successfully generates the commanded voltage at different frequencies. Any loss in the output voltage due to loading and device voltages with finite currents can be compensated for in closed-loop.

- The input and the output currents are nearly sinusoidal as intended:
  - The second-order input current filter of Table 2.11 used with the I-type topology attenuates the switching frequency (and higher) components of the input

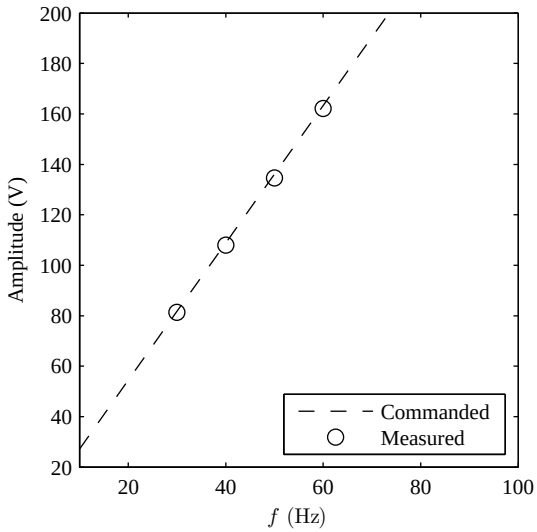


Figure 2.42: Open-circuit voltage generated by the I-type indirect matrix converter based open-end winding drive.

current to $< 1\%$ as seen in Fig. 2.40(b), and,

– the significantly smaller third-order input current filter of Table 2.11 used with the T-type topology also attenuates the switching frequency (and higher) components of the input current to $< 1\%$ as seen in Fig. 2.41(b).

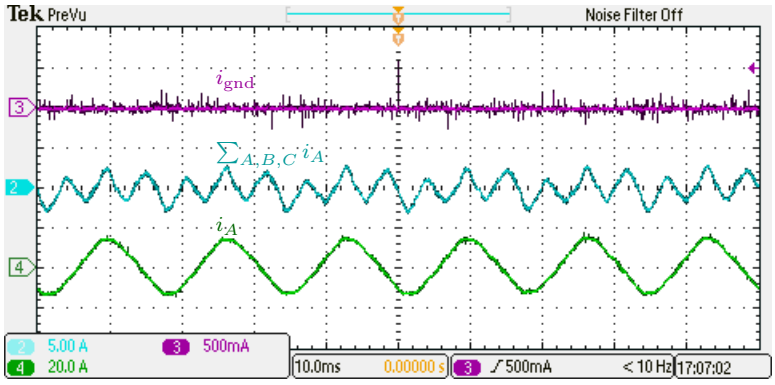
This validates the assertion that performance similar to a second-order filter can be achieved using a significantly smaller third-order filter; thus further shrinking the size of the reactive components required by matrix converters.

- While the switching frequency (and higher) harmonics are not present in the input currents (in Figs. 2.39(a), (b), 2.40(b), 2.41(b)), lower order harmonics are observed.

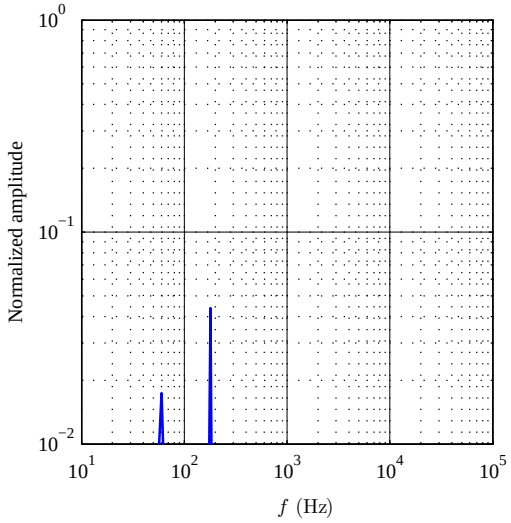
- Lower order harmonics ($> 1\%$) are also observed in the output current with the motor load (Figs. 2.39(a), 2.40(d)). These harmonics are also present with the RL load (Fig 2.41(d)) but the magnitude is small ($< 1\%$). The presence of odd-triplen harmonic current in open-end winding drives is known in literature [79]: a low-frequency common-mode current at odd-triplen harmonics of the output fundamental frequency circulates between the two sets of terminals. This current is caused by the difference between the common-mode voltages at the two sets of terminals. While ideally the common-mode voltage is zero at both sets of terminals, due to the device voltage drops and the finite blanking time (dead time) used for safe switching, a small common-mode voltage appears. Since the common-mode impedance of the motor is low ($R_s + jX_{ls}$), the current is large (compared to an RL load) as observed from Figs. 2.40(d) and 2.41(d).

  Fig. 2.43(a) shows the waveform of the common-mode current along with its spectrum in Fig. 2.43(b) for the conditions of Fig. 2.39(a). The common-mode current was measured using a Rogowski probe of bandwidth 1 MHz — therefore the spectrum is reliable only at low frequencies. The low-frequency common-mode current (circulating current) explains part of the distortion in the motor current. The root cause of other low-frequency harmonics is under investigation.

- The low-frequency harmonics in the input current are discussed later in this section.



(a) The common-mode current



(b) Spectrum of the common-mode current

Figure 2.43: Common-mode current drawn by the open-end winding machine.

Power factor control

When the power factor control parameter $\alpha = 0.5$, the switching cycle averaged current drawn by the drive is in phase with the input voltage (unity power factor). For $\alpha > 0.5$, the current drawn by the drive lags the input voltage and for $\alpha < 0.5$, it leads the input voltage.

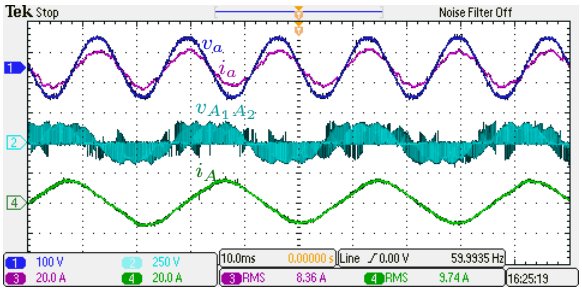
The total grid current is the sum of the input current synthesized by the drive and the current drawn by the filter capacitor. Since the capacitor draws a leading current,

the power factor control parameter needs to be adjusted for the drive to draw current in phase with the input voltage. E.g. in Fig. 2.39(a), $\alpha = 0.6$ results in ∼upf input. In Fig. 2.39(b), the input current lags the input voltage at $\alpha = 0.7$.

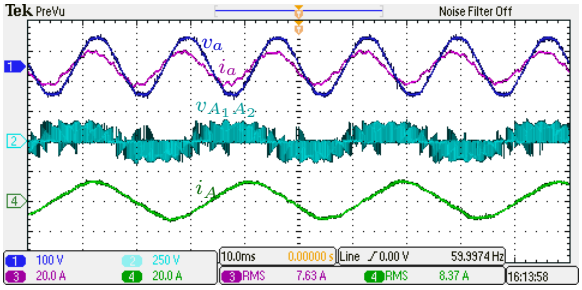
Few more results demonstrating the power factor control at lower output frequencies are shown in Figs. 2.44 and 2.45 for the I-type topology, but the results also apply to the T-type topology.

Intelligent commutation and clamp circuit-less operation

The prototypes described in a previous section do not use any clamp circuit. A path always exists for the inductive load currents and the source currents into the filter capacitors through the antiparallel diodes of the IGBTs. All results shown in this dissertation are without any additional clamp diodes or capacitors.

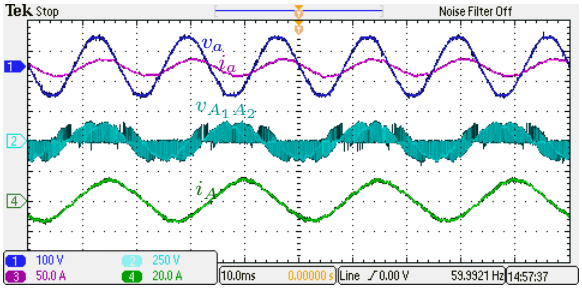


(a) $\alpha = 0.70$ (somewhat lagging)

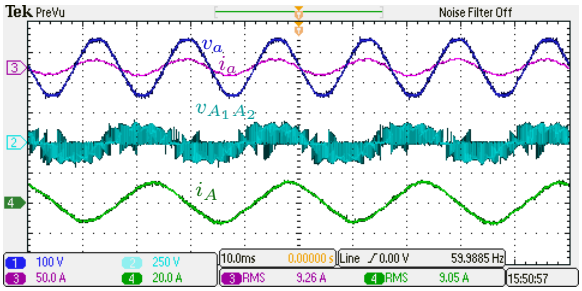


(b) $\alpha = 0.30$ (somewhat leading)

Figure 2.44: Operation at different α for power factor control at $f_{\text{out}} = 35\,\text{Hz}$. Input voltage $\approx 122\,\text{V}$, switching frequency $\approx 10\,\text{kHz}$. Output voltage is set according to the output frequency and $V/f = 200/60\,(\text{V/Hz})$.



(a) $\alpha = 1.0$ (lagging to the limit)



(b) $\alpha = 0.40$ (somewhat leading)

Figure 2.45: Operation at different α for power factor control at $f_{\text{out}} = 40\,\text{Hz}$. Input voltage $\approx 122\,\text{V}$, switching frequency $\approx 10\,\text{kHz}$. Output voltage is set according to the output frequency and $V/f = 200/60\,(\text{V/Hz})$.

Fig. 2.46 shows the output voltage waveforms at the terminals A_1 and A_2, and the phase voltage $v_{A_1A_2}$ measured across these terminals. The voltage at the terminal A_1 is being held fixed and the voltage at the terminal A_2 is being switched according to the pattern $v_{A_2} = v_{\text{max}}, v_{\text{mid}}, v_{\text{min}}, v_{\text{mid}}, v_{\text{max}}, \ldots$

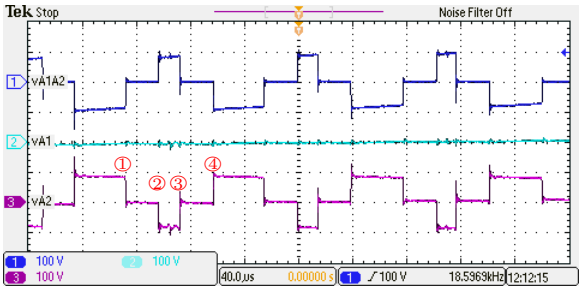


Figure 2.46: Intelligent commutation.

Let us focus on the transitions $v_{\max} \leftrightarrow v_{\text{mid}}$ marked ① and ④ in Fig. 2.46. The transitions are automatically intelligent when i_A enters the terminal A_2 (since turning all IGBTs off would clamp the voltage v_{A_2} to $v_{\max}$). When i_A leaves the terminal A_2, in the absence of intelligent commutation, a glitch to the voltage $v_{\min}$ would have been observed. Of course, no such glitch is seen at the transitions ① and ④ in Fig. 2.46.

Similarly, for i_A leaving the terminal A_2, the transitions ② and ③ are automatically intelligent. However, in the absence of intelligent commutation, a glitch to the voltage $v_{\max}$ would have been observed at transitions ② and ③ when current enters the terminal A_2. No glitch at any of the four transitions verifies intelligent commutation for $i_A \lesseqgtr 0$.

2.5.3 Sources of distortion in the input current

It was seen earlier that low-frequency harmonics could be present in the output current, especially with a motor load. Since the input current is synthesized from the output current, some of these harmonics may make their way into the input. However, were that to be the only cause, the input current would not have any low-frequency harmonics with an RL load that has an almost sinusoidal output current (Fig. 2.39(b)). Yet low-frequency harmonic content is observed in the input current (Figs. 2.39(b) and 2.41(b)).

Part of the low-frequency content in the input current is simply the harmonic current drawn by the filter capacitors from the input supply — since the input supply has low-frequency harmonics (Figs. 2.40(a), 2.41(a)), and the admittance offered by the capacitors increases with frequency, the harmonic content in the current appears amplified. Fig. 2.47 shows the input voltages and the current drawn by the front- end converter with the load-end converters switched OFF. Significant harmonic current is seen. If the current harmonics are caused because of the input voltage distortion, then they should be present in simulation with the same voltages as Fig. 2.47. Furthermore, the harmonics must disappear when the input voltages are changed to ideal sinusoids — Fig. 2.48(a) shows the simulated front-end current with the voltage data of Fig. 2.47 and Fig. 2.48(b) shows the front-end current with sinusoidal voltage sources. The harmonic current is present with the real voltages in Fig. 2.48(a) whereas the input current is sinusoidal with the ideal sources in Fig. 2.48(b).

Therefore, the harmonic content in the input voltage is a source of harmonics in the input current. The other sources of distortion are the low-frequency harmonics in the

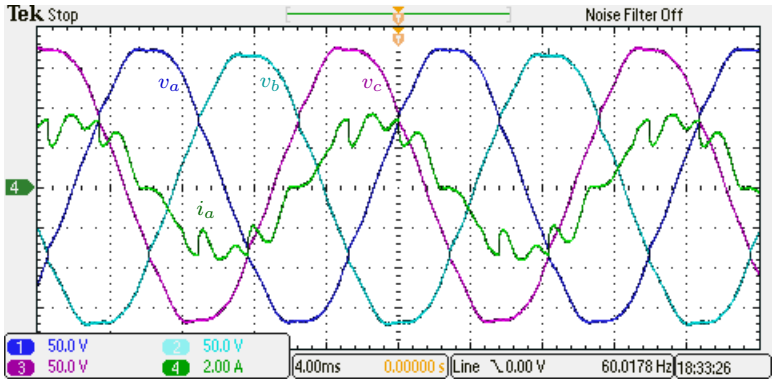
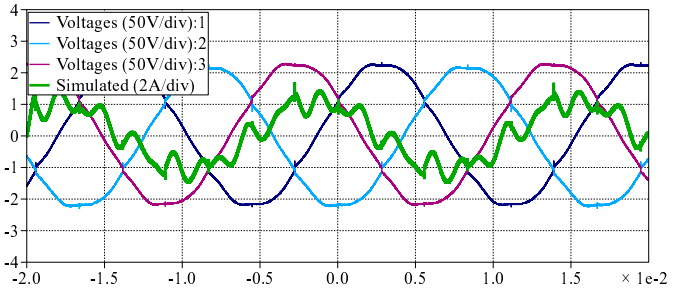
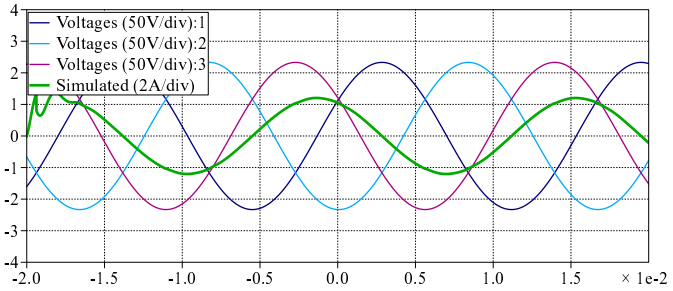


Figure 2.47: Current drawn by the front-end converter along with the input voltages.



(a) Simulation with real voltages



(b) Simulation with ideal voltages

Figure 2.48: Front-end simulation with (a) real voltages and (b) ideal voltages. V/div and A/div same as Fig. 2.47. A scope-like format is used for consistency with Fig. 2.47.

load current and the amplification of lower sidebands of f_{sw} by the grid current filter. The root cause of low-frequency distortion in the output current is under investigation. It is expected that addressing the output current harmonics would also remedy the input current distortion.

2.6 Summary

In summary, this chapter introduced matrix converter based open-end winding drives for output common-mode voltage elimination and described their development. The theory of operation of the indirect matrix converter based open-end winding drive and the possible topologies (I-type and T-type) were discussed. Output voltage synthesis and input current synthesis with power factor control were described. It was shown qualitatively that the direct and the indirect matrix converter based open-end winding drives operate on the same principle.

A third-order filter for filtering the grid current was designed and optimized to limit the amplification of non-fundamental frequencies. It was shown that attenuation similar to a conventional second-order filter can be obtained using much smaller components in this third-order filter.

The operating principle of the indirect matrix converter based open-end winding drives was verified using experimental results from the prototypes of both indirect topologies (I-type and T-type). These prototypes were also used to validate the superiority of the third-order filter designed in this chapter. High voltage transfer ratio, input power factor control, clamp circuit-less operation, and intelligent commutation were demonstrated.

Loss-optimal switching sequences were proposed for direct and indirect matrix converter based open-end winding drives. The verification of lower losses with the proposed sequences is left for the next chapter. The discussion of the common-mode performance of the presented drives is reserved for Chapter 4.

Sources of distortion in the input and the output currents were identified. Further causes of low-frequency distortion in the currents are under investigation.

Chapter 3

Matrix converter based open-end winding drives: part 2

The operation of direct and indirect matrix converter based open-end winding drives for common-mode elimination was discussed in the last chapter. It was shown that the direct and the indirect topologies operate on the same principle of synthesizing the output voltage vector from synchronously rotating vectors to eliminate the common-mode voltage and to control the input power factor while offering a superior voltage transfer ratio compared to conventional matrix converter based drives.

A filter design applicable to all three topologies (one direct and two indirect) was discussed and its advantages over a conventional second-order filter were shown quantitatively. A switching strategy to minimize the losses by minimizing the number of switching transitions was discussed qualitatively.

The advantages of the indirect approach were discussed and the experimental validation of its capabilities was provided for both of the indirect topologies. Experimental results for the direct approach have already been published by Gupta [62–64].

A framework for the calculation of the semiconductor losses would be laid in this chapter. This framework would be used to validate the loss-optimal switching strategy that was discussed in the previous chapter. The validity of the proposed third-order filter has already been established in the previous chapter.

The results reported in the previous chapter utilized a triangular carrier for the pulse

width modulation. An alternative carrier would be investigated for possible advantages.

With a common input filter, a common carrier and switching strategy, and a loss calculation framework in place, the three matrix converter based open-end winding (OE Wdg.) drive topologies would be compared against each other to identify the best matrix converter based open-end winding drive. The comparison will include semiconductor requirements, semiconductor losses, and the quality of the input and the output waveforms.

3.1 A loss calculation framework

Insulated gate bipolar transistors (IGBTs) and fast recovery diodes are the semiconductor devices commonly used in drives applications. The semiconductor losses in a drive consist of the conduction losses due to the collector-emitter saturation voltage ($V_{CE,\text{sat}}$) of the IGBTs, forward voltage (V_F) of the diodes; and the switching losses due to the turn-ON energy and the turn-OFF energy of the IGBT ($E_{\text{ON}}, E_{\text{OFF}}$), and the reverse recovery energy of the diode (E_{RR}).

The voltages $V_{CE,\text{sat}}, V_F$ depend upon the gate-emitter voltage and the junction temperature. The energies $E_{\text{ON}}, E_{\text{OFF}}, E_{\text{RR}}$ depend upon the gate-emitter voltage, the gate resistance, the voltage and the current being switched, and the junction temperature.

The dependence of these variables against the operating conditions (bus voltage, collector current, junction temperature, gate-emitter voltage, gate resistance) is often published in the datasheet for the estimation of the semiconductor losses.

Consider a phase leg of a matrix converter shown in Fig. 3.1. For simplicity, only two input phases are shown even though in general, an output phase will alternately be connected to three input phases in the drives being discussed. The output current i_M is sourced from the input voltage v_i when the duty cycle signal D_{iM} is active and from input voltage v_j when the duty cycle signal D_{jM} is active. Let d_{iM}, d_{jM} be the duty ratios corresponding to the duty cycle signals D_{iM}, D_{jM}. The conduction losses are:

$$E_{\text{conduction}} = i_M \times (d_{iM} T_{\text{sw}} + d_{jM} T_{\text{sw}}) \left(V_{CE,\text{sat}}(i_M) + V_F(i_M)\right) \tag{3.1}$$

The energy lost at the first switching transition ($D_{iM} = 0 \rightarrow D_{iM} = 1$) is:

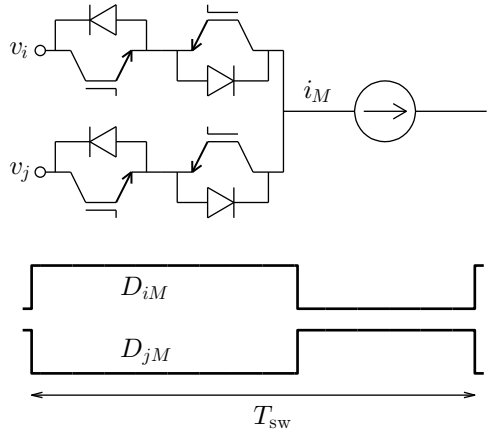


Figure 3.1: Illustration of the semiconductor loss calculation.

$$E_{\text{sw},1} = \overline{((v_{ij} \geq 0) \oplus (i_M \geq 0))} \times (E_{\text{ON}}(|v_{ij}|, |i_M|) + E_{\text{RR}}(|v_{ij}|, |i_M|)) + ((v_{ij} \geq 0) \oplus (i_M \geq 0)) \times E_{\text{OFF}}(|v_{ij}|, |i_M|) \tag{3.2}$$

The energy lost at the second switching transition ($D_{iM} = 1 \rightarrow D_{iM} = 0$) is:

$$E_{\text{sw},2} = ((v_{ij} \geq 0) \oplus (i_M \geq 0)) \times (E_{\text{ON}}(|v_{ij}|, |i_M|) + E_{\text{RR}}(|v_{ij}|, |i_M|)) + \overline{((v_{ij} \geq 0) \oplus (i_M \geq 0))} \times E_{\text{OFF}}(|v_{ij}|, |i_M|) \tag{3.3}$$

The total energy lost in one T_{sw} cycle is:

$$E_{\text{semiconductor},T_{\text{sw}}} = E_{\text{conduction}} + E_{\text{sw},1} + E_{\text{sw},2} \tag{3.4}$$

A summation of $E_{\text{semiconductor},T_{\text{sw}}}$ over a sufficiently large number of switching cycles can be used to calculate the average power loss:

$$P_{\text{loss, semiconductor}} = \frac{1}{nT_{\text{sw}}} \sum_{k=1}^{n} E_{\text{semiconductor},T_{\text{sw}}}[k] \tag{3.5}$$

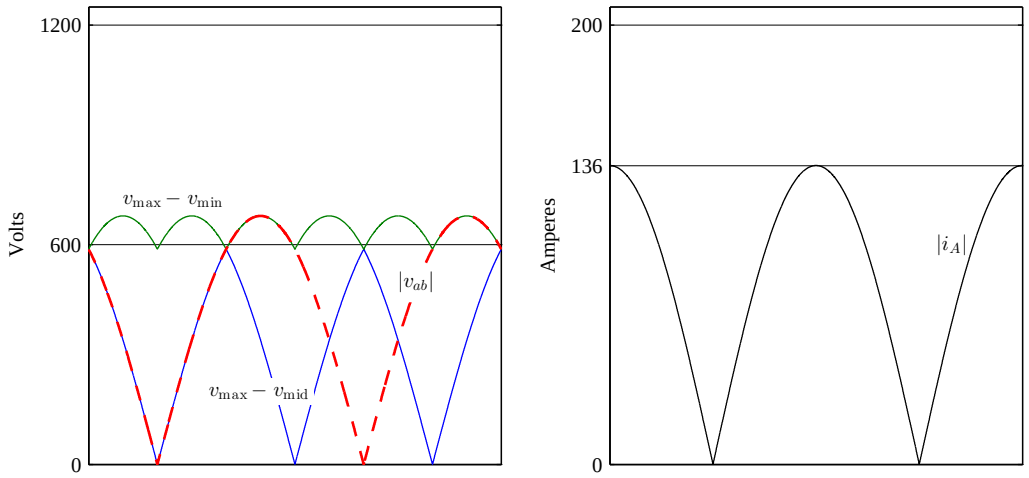
The dependance of $V_{CE,\text{sat}}, V_F, E_{\text{ON}}, E_{\text{OFF}}, E_{\text{RR}}$ on the gate-emitter voltage, the gate resistance, and the junction temperature is implicit in the equations above. The loss calculation for all three of the matrix converter based open-end winding drives follows an extension of the procedure described above.

3.1.1 The system and the devices used

For comparison of the different matrix converter based open-end winding drive topologies against each other, a system ($V_{\text{base}}, S_{\text{base}}$) needs to be selected first. A 480 V, 80 kVA system is chosen for comparison since it is representative of a wide range of industrial drives. The base current for this system is $I_{\text{base}} = 96.22\,\text{A}$.

Fig. 3.2 illustrates the voltage and the current ratings required of the semiconductor devices for this drive. For a direct matrix converter based open-end winding drive, the switches need to be able to block the peak line-to-line voltage. For the T-type indirect matrix converter drive, the half-bridge IGBTs and diodes need to block the peak line-to-line voltage whereas the IGBTs (and diodes) of the four-quadrant switch need to block the peak of the voltage $v_{\text{max}} - v_{\text{mid}}$. For the I-type topology, the devices need to block the peak of the voltage $v_{\text{max}} - v_{\text{mid}}$ if the optimal switching sequence proposed in the last chapter is used. However, if there is a possibility of $v_{\text{max}} \leftrightarrow v_{\text{min}}$ transitions, then the IGBTs and the diodes must be able to block the peak line-to-line voltage. All IGBTs and diodes must be able to conduct the peak phase current ($= \sqrt{2} I_{\text{base}}$).

The semiconductor devices are typically used only up to 50%–67% of their ratings in order to maintain a margin of safety. IGBTs and diodes for drive applications are typically rated at 600 V, 1200 V and 1700 V. Respecting the margin of safety, the IGBT



(a) Voltage ratings (b) Current ratings

Figure 3.2: Voltage and current ratings required.

module CM200DU-24NFH (1200 V, 200 A) from Powerex, Inc. is used for this analysis.

Following data is available from the device datasheet:

- $V_{CE,\text{sat}}$ as a function of the collector current at 25 °C and 125 °C.
- V_F as a function of the emitter current at 25 °C and 125 °C.
- $E_{\text{ON}}, E_{\text{OFF}}, E_{\text{RR}}$ as a function of the collector/emitter current at 125 °C and 600 V.
- IGBT and diode transient thermal impedance.

Following assumptions are made:

- $E_{\text{ON}}, E_{\text{OFF}}, E_{\text{RR}}$ are assumed to be independent of temperature since the data is specified only at 125 °C.
- $E_{\text{ON}}, E_{\text{OFF}}, E_{\text{RR}}$ are directly proportional to the voltage switched since the data is specified only at 600 V.
- $V_{CE,\text{sat}}, V_F$ at temperatures other than 25 °C and 125 °C are found by linear interpolation.
- The gate voltage and the gate resistor are same as the ones at which the data is specified in the datasheet.
- The transient thermal impedance can be represented by a first order circuit.
- For simplification, the IGBT thermal impedance is also used for the diode.
- The heat sink is an isothermal sink with ~ 0 thermal impedance (to the ambient); and the ambient is at a constant temperature of 25 °C.

Under the assumptions above, simulations were run for an idealized Buck converter circuit at several operating points and the results were found to be in good agreement with the manufacturer's loss estimation software (Table 3.1). The IGBT losses (switching and conduction) calculated in the simulations matched with the manufacturer's software within $\sim 5\%$ or better at all operating points except one. The diode switching losses matched with the manufacturer's software within $\sim 10\%$ or better at all operating points, but the diode conduction losses had higher errors.

	IGBT switching (W)		IGBT conduction (W)	
	Manufacturer's software	Simulated	Manufacturer's software	Simulated
OP1	102	101	159	168
OP2	130	130	466	464
OP3	65	65	466	466
OP4	100	99	26	30
	Diode switching (W)		Diode conduction (W)	
	Manufacturer's software	Simulated	Manufacturer's software	Simulated
OP1	132	121	87	103
OP2	166	155	78	88
OP3	83	78	78	92
OP4	124	116	50	61
	IGBT T_j(°C)		Diode T_j(°C)	
	Manufacturer's software	Simulated	Manufacturer's software	Simulated
OP1	59	65	74	59
OP2	98	114	88	62
OP3	89	105	67	50
OP4	43	44	64	52

Table 3.1: Comparison of the losses calculated in the simulation against the manufacturer's software for IGBT CM200DU-24NFH. OP1 ... OP4 are some operating points.

Errors as high as $\sim 25\,^{\circ}\mathrm{C}$ were seen in the estimation of the junction temperature. This is attributed to the use of the same junction to case thermal impedance for the IGBT and the diode — the IGBT junction temperatures were overestimated whereas the diode junction temperatures were underestimated. It is possible that the errors in the junction temperature estimation cause the errors in the diode conduction losses. It must be noted that the simplified simulation model is not an accurate thermal representation of the physical device in the first place. Therefore, with reasonable agreement with the manufacturer's software, the simulation model is deemed satisfactory for the calculation of the losses. It is understood that the predicted junction temperatures are more of an indicator of the calculated losses, and not the accurate estimates of the actual junction temperature.

3.2 Simulation of the DMC OE Wdg. drive

This section describes the procedure and presents the results of the simulation of the direct matrix converter (DMC) based open-end winding (OE Wdg.) drive with semiconductor loss calculations for the system chosen (480 V, 80 kVA).

3.2.1 Operating points used

The simulations are run at the switching frequencies 6 kHz, 12 kHz, 18 kHz, and at power factor control parameters $\alpha = 0$ (leading), $\alpha = 0.5$ (unity power factor), and $\alpha = 1$ (lagging). Simulations are run with a triangular carrier and a sawtooth carrier to analyze the effect of the carrier on the semiconductor losses and on the input current and the output voltage distortion. The third-order filter design of Table 2.10 is used for the input current filter.

To expedite the simulations, an RL load is used instead of a motor load. The impedance of the load is fixed at $Z_{\text{base}}\angle\phi$ where $\phi : \cos\phi = 0.8, \phi > 0$. Therefore the inductance is a function of the output frequency; while unrealistic for a passive load, this load is used so that the magnitude of the impedance and the power factor control range don't change with the output frequency. The output frequency is varied from 15 Hz to 75 Hz in steps of 15 Hz. The output voltage is set according to a V/f control law:

$$V_{\text{out}} = \frac{f_{\text{out}}}{f_{\text{base}}} V_{\text{base}} \tag{3.6}$$

where $f_{\text{base}} = 60\,\text{Hz}$. The power drawn by this load at different operating points is shown in Fig. 3.3. The expected power-frequency characteristic is also shown.

A total of 90 simulations at 3 different switching frequencies, 3 different input power factors, 5 different load conditions, and 2 different carriers are run. It is neither practical, nor necessary, to discuss the waveforms for every single operating point. Waveforms for one operating point are shown and it is understood that the waveforms from the other operating points are similar.

Let the switching frequency f_{sw} be 6 kHz. Let the power factor control parameter α be equal to 1. Let the output frequency f_{out} be 75 Hz. The output voltage is determined from (3.6). Let the carrier be triangular. Fig. 3.4 shows the input and the output

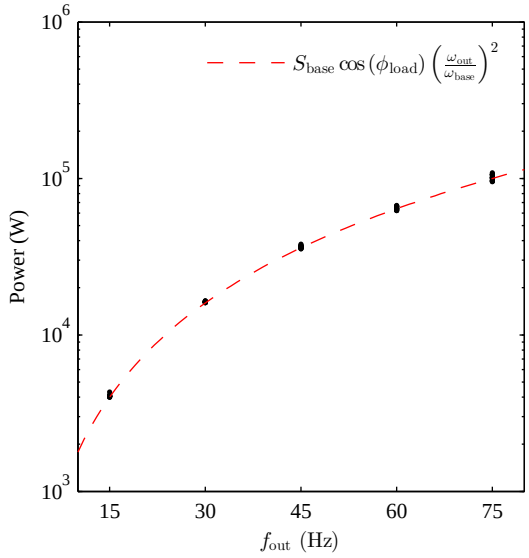
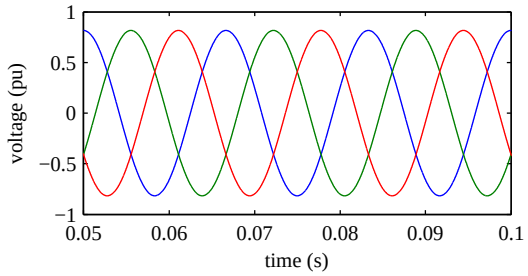


Figure 3.3: Output power as a function of the output voltage frequency.

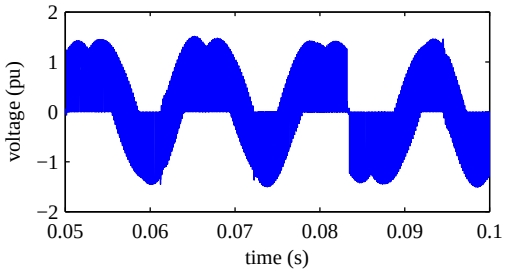
voltages and currents at this operating point. The common-mode voltage is also shown. As expected, the input and the output currents are sinusoidal and the common-mode voltages at both sets of terminals is zero.

It must be mentioned that the chosen IGBT/diode would be inadequate at this operating point, and at all operating points with $f_{\text{out}} = 75\,\text{Hz}$, since the input current would exceed the device rating at its peak value. However, the conclusions drawn from these hypothetical operating points ($f_{\text{out}} = 75\,\text{Hz}$) are still useful in identifying the patterns in the semiconductor losses and input/output waveform quality.

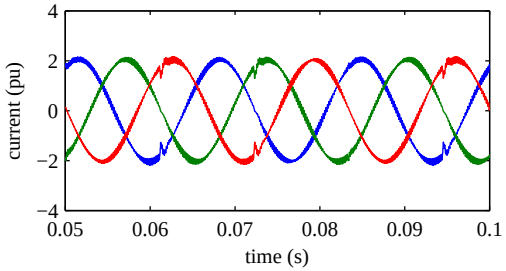
The semiconductor losses and the estimated junction temperatures for this operating point are shown in Fig. 3.5. Since only one set of vectors is used for output voltage synthesis ($\alpha = 1$), the switching losses in the converters vanish alternately.



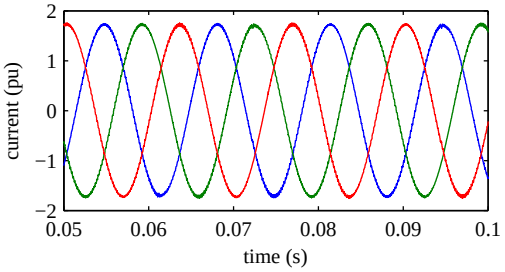
(a) Input voltages v_a, v_b, v_c



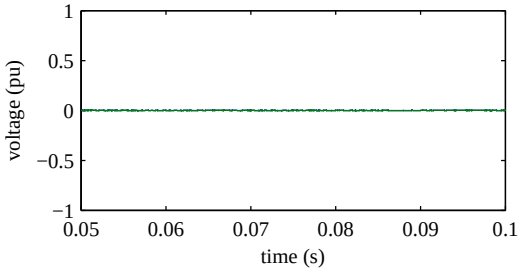
(b) Output voltage $v_{A_1A_2}$



(c) Input currents i_a, i_b, i_c

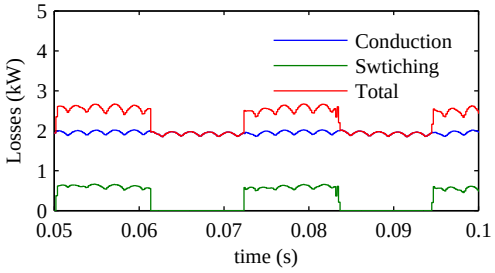


(d) Output currents i_A, i_B, i_C

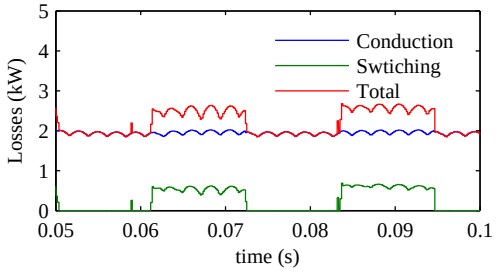


(e) Common-mode voltages $v_{\mathrm{CM}_1}, v_{\mathrm{CM}_2}$ at both sets of terminals

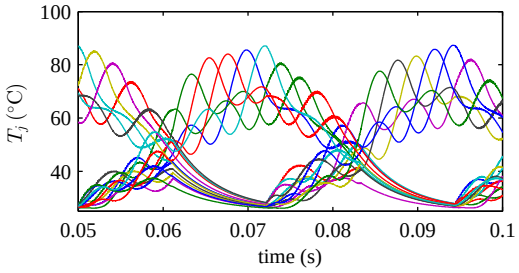
Figure 3.4: Simulation results of the DMC based OE Wdg. drive: input/output waveforms for the operating point $f_{\mathrm{sw}} = 6\,\mathrm{kHz}, \alpha = 1, f_{\mathrm{out}} = 75\,\mathrm{Hz}$ with triangular carrier.



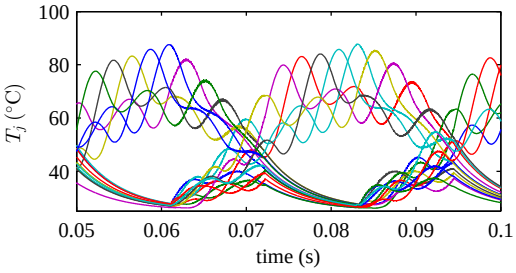
(a) Losses in the first matrix converter



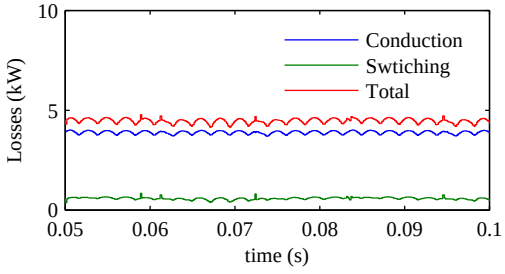
(b) Losses in the second matrix converter



(c) Junction temperatures of the first matrix converter



(d) Junction temperatures of the second matrix converter



(e) Total losses in the two converters

Figure 3.5: Simulation results of the DMC based OE Wdg. drive: semiconductor losses and junction temperatures for the operating point of Fig. 3.4.

3.2.2 Effect of the carrier

In three-phase voltage source inverters (VSIs), a switch turns ON and OFF once every switching cycle independent of the carrier used (sawtooth or triangular). However, a triangular carrier eliminates the dominant switching frequency harmonic in the output line-to-line voltage. Therefore a triangular carrier is almost always used [2].

The advantages of using a triangular carrier, however, are not certain in the presented drives. It will be shown in a later section that the switching strategy proposed in the previous chapter does in fact reduce the switching losses. Assuming, for now, that this is indeed the case, the switching sequences for one direct matrix converter of the open-end winding drive with a triangular carrier and a sawtooth carrier are shown in Fig. 3.6.

The number of the switching transitions in one switching cycle is clearly lower with a sawtooth carrier, which may translate into lower switching losses. Therefore if the triangular carrier does not offer significant reduction in the harmonics, it may be better to use a sawtooth carrier.

The spectrum of the output voltage $v_{A_1A_2}$ of Fig. 3.4 is shown in Fig. 3.7. The spectrum at the same operating point, but with a sawtooth carrier, is also shown. Spectra of the input current at similar conditions (same operating point, different carriers) are shown in Fig. 3.8. The most stringent limits set forth in IEEE 519-1992 [80] are also marked in the low-frequency detail of the input current spectra.

While the spectra with different carriers are different, it cannot be concluded if one carrier is necessarily better than the other. Therefore further investigation would be

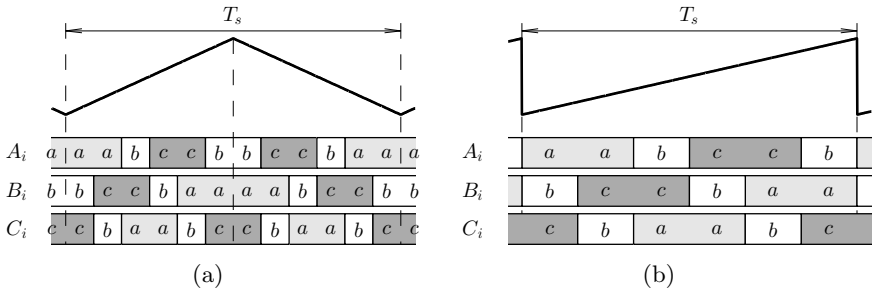
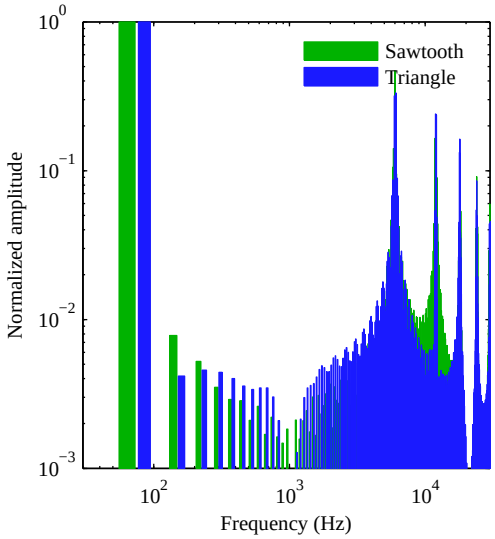
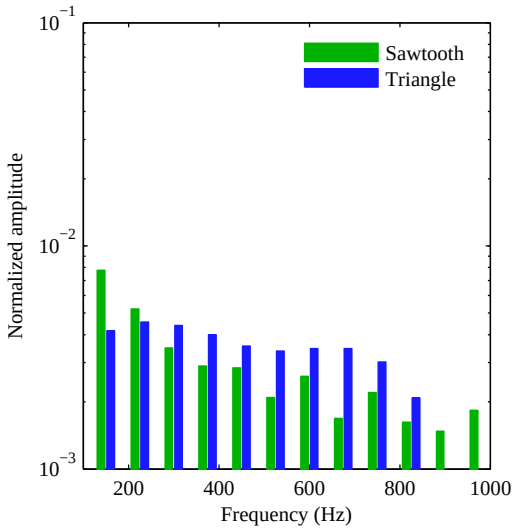


Figure 3.6: Vector sequences for a direct matrix converter of the DMC OE Wdg. drive for (a) triangular and (b) sawtooth carriers.

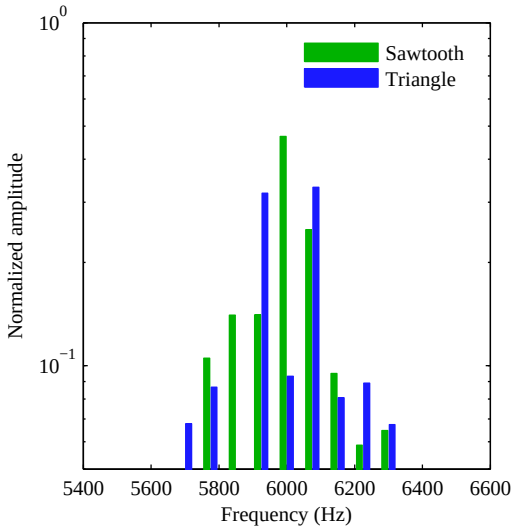
conducted across all operating points and topologies to determine the more suitable carrier.



(a) Entire range

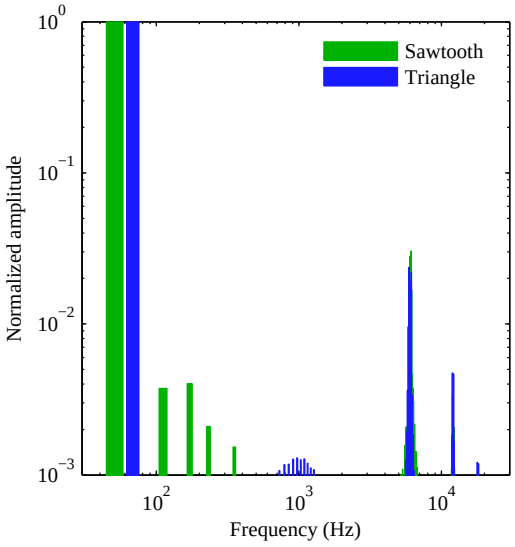


(b) Low-frequency

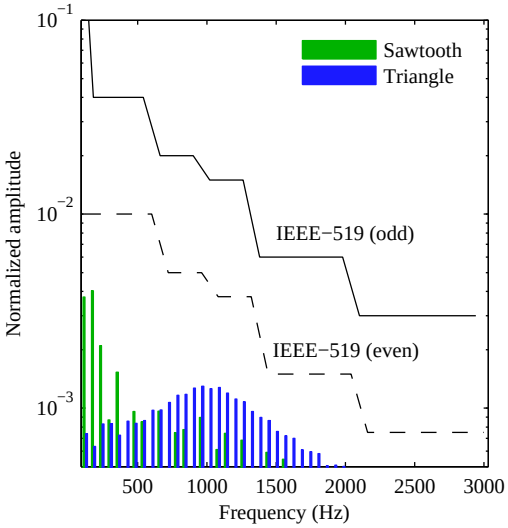


(c) Sidebands of f_{sw}

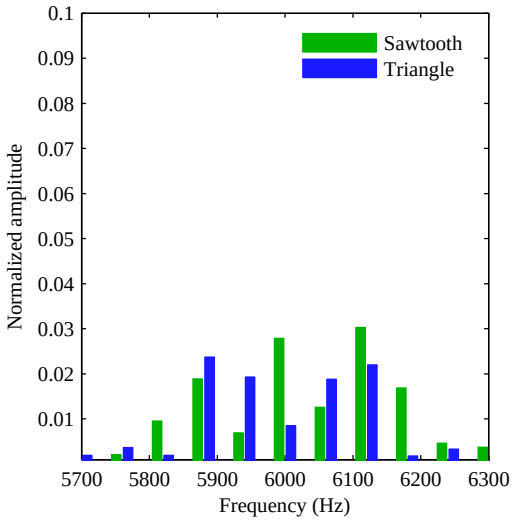
Figure 3.7: Spectra of the output voltage for different carriers at the same operating point.



(a) Entire range



(b) Low-frequency



(c) Sidebands of f_{sw}

Figure 3.8: Spectra of the input current for different carriers at the same operating point.

3.2.3 Waveform quality

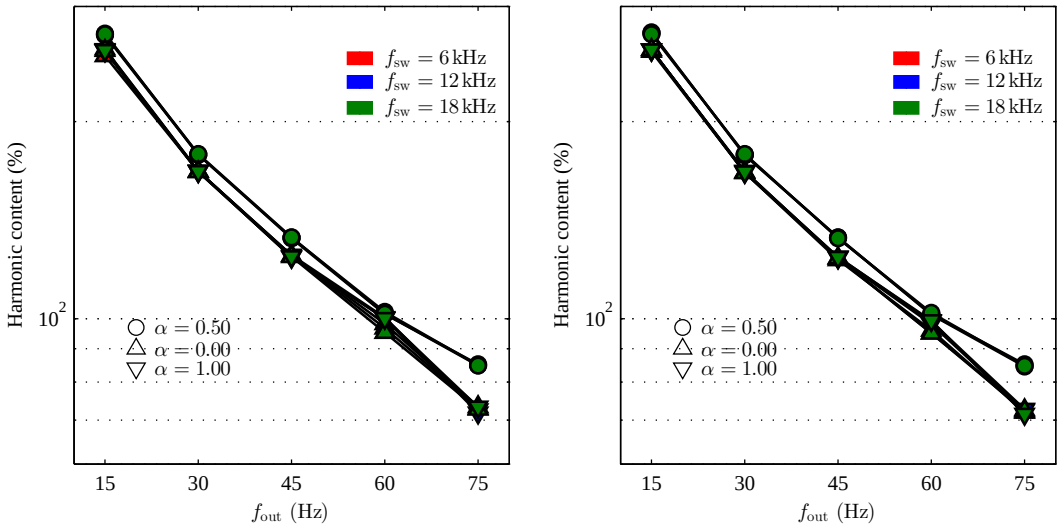
The harmonic content in the output voltage and the input current across all operating points for different carriers is shown in Figs. 3.9 and 3.10 respectively. The harmonic content is defined as:

$$\text{Harmonic content} = \sqrt{\sum_{h\neq 1}\left(\frac{x_h}{x_1}\right)^2} \tag{3.7}$$

where h is the harmonic order and x is either the voltage or the current [11].

Although the harmonic content defined above is generally known as total harmonic distortion (THD) [11], the use of the term THD is being avoided on purpose to avoid confusion with THD as defined in [80] that considers harmonics only up to the 50^{th} order for THD calculation.

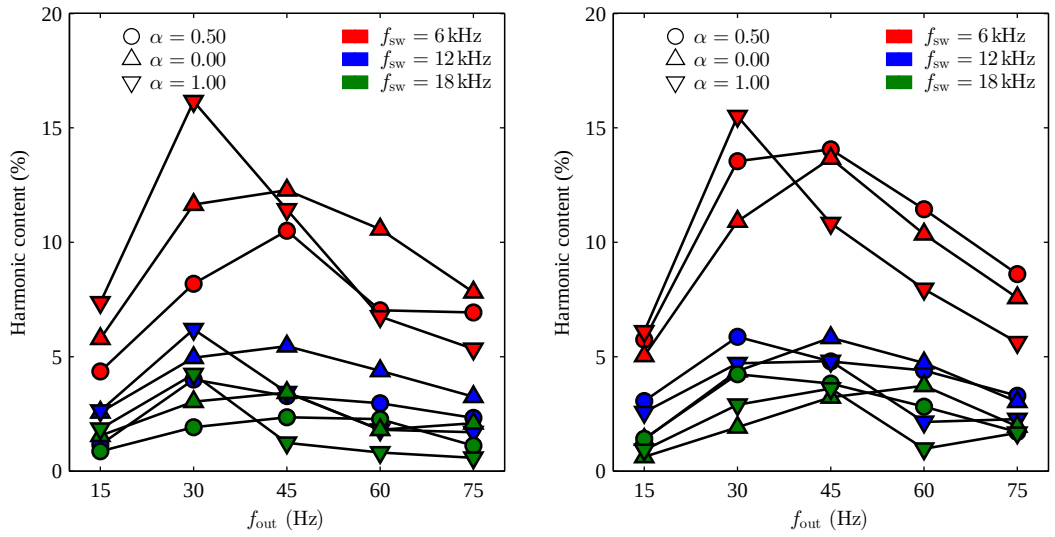
The harmonic content in the output voltage is independent of the switching frequency and the carrier used. If the switching frequency is sufficiently larger than the output frequency, the independence of the output voltage harmonic content from the switching frequency is expected. Similar harmonic content with triangular and sawtooth carriers, however, is an important result and will prove useful in determination of the



(a) Triangular carrier

(b) Sawtooth carrier

Figure 3.9: Harmonic content in the output voltage.



(a) Triangular carrier

(b) Sawtooth carrier

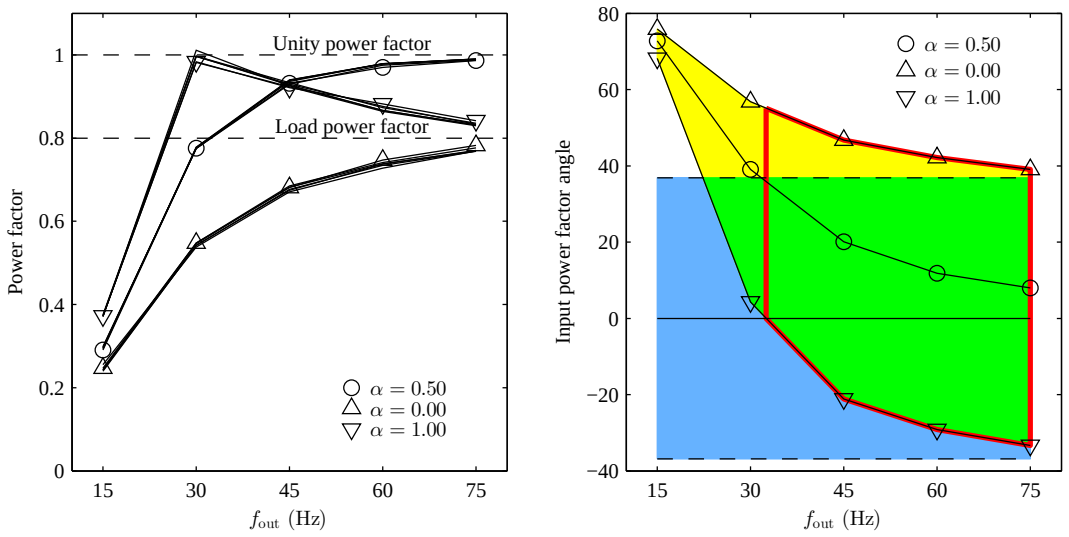
Figure 3.10: Harmonic content in the input current.

most suitable carrier.

In case of the input current, a clear reduction in the harmonic content is seen as the switching frequency is increased. This is expected because the filter offers a higher attenuation as the switching frequency increases. The relationship between the harmonic content and the carrier is, once again, not definite. However, the harmonic content at $\alpha = 0.5$ is consistently lower with a triangular carrier — it is generally desirable to operate at unity power factor and the lower harmonic content offered by the triangular carrier at $\alpha = 0.5$ favors the use of this carrier.

3.2.4 Power factor control

Since the load power factor is 0.8 (lagging), $\alpha = 0$ should yield an input power factor of 0.8 (leading), $\alpha = 0.5$ should yield unity input power factor, and $\alpha = 1$ should yield an input power factor of 0.8 (lagging). The leading current drawn by the input filter capacitor, however, affects the power factor angle. This is shown in Fig. 3.11(a) for all operating points. The input power factor approaches its intended value as the load increases and the filter capacitor current becomes smaller in comparison to the fundamental current drawn by the drive.



(a) Input power factor at all operating points

(b) Input power factor control range with filter capacitors

Figure 3.11: Input power factor control.

The effect of the input capacitor on the power factor control range is illustrated in Fig. 3.11(b): the blue region is the ideal power factor control range and the yellow region is the range in which the power factor can be controlled in presence of the input filter capacitor. The green region is the intersection of the two. The region enclosed in red represents the values of the load for which the power factor can be controlled to unity.

3.2.5 Semiconductor losses

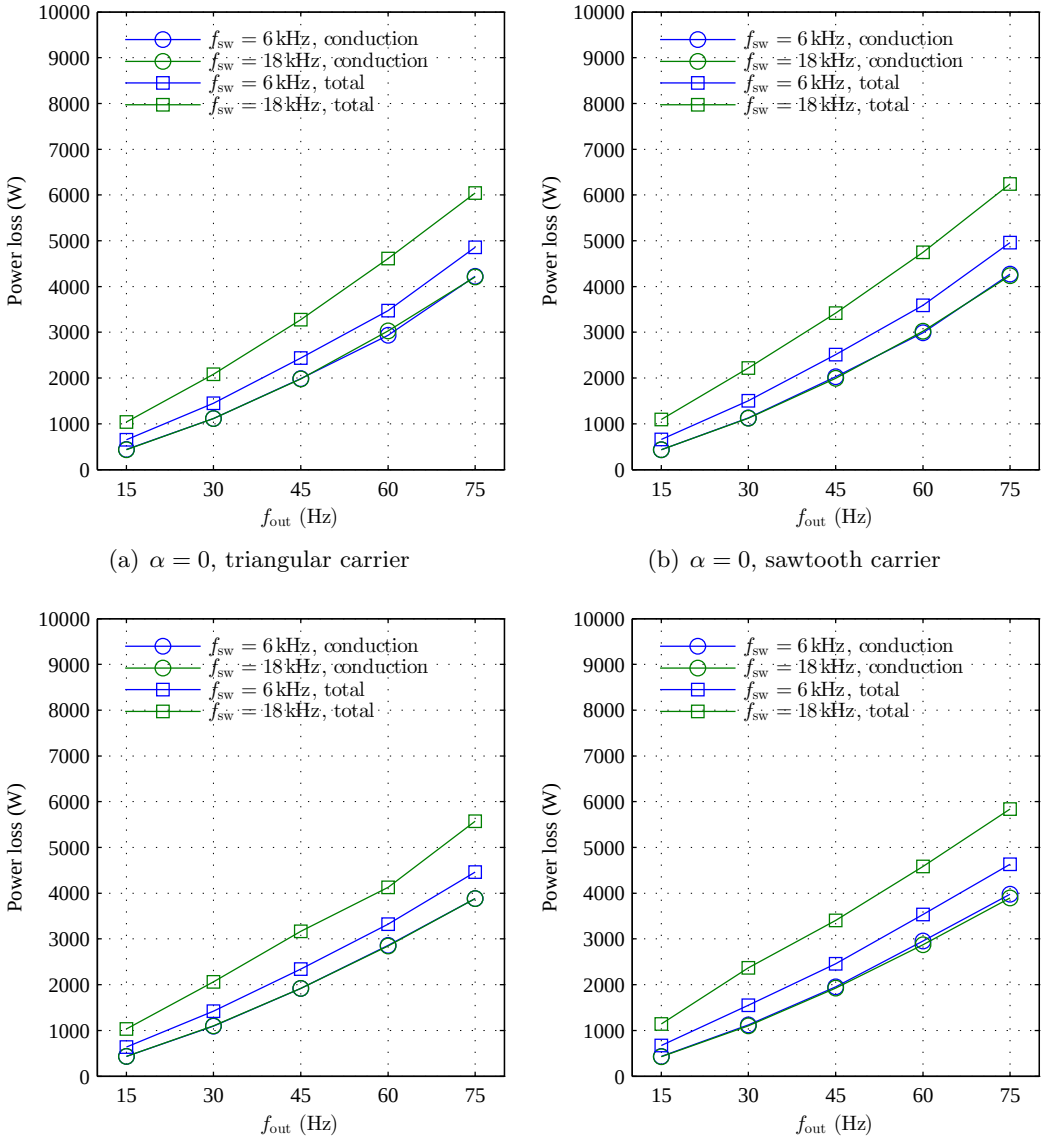
The semiconductor losses for the direct matrix converter based open-end winding drive are calculated using the procedure described earlier in this chapter. The losses are calculated at different switching frequencies and at different values of the input power factor control parameter α. Both, triangular and sawtooth, carriers are used to examine the effect of the carrier on the losses.

The losses for $\alpha = 0$ and $\alpha = 1$ are shown in Fig. 3.12. The losses for $\alpha = 0.5$ (upf) are shown in Fig. 3.13. As expected, the choice of the carrier and the switching frequency don't affect the conduction losses. The switching losses (difference between

the conduction losses and the total losses) increase in proportion to the switching frequency. The total losses with the triangular carrier and the sawtooth carrier are similar when only one set of vectors is used ($\alpha = 0, 1$) due to the following factors:

- The losses are dominated by the conduction losses that are independent of the carrier,
- the switching losses are incurred only in one converter at a time (Fig. 3.5(a)),
- and in the converter that incurs switching losses, the number of transitions with a triangular carrier is only slightly higher than that with a sawtooth carrier.

In the general case when both sets of vectors are used, the difference in the number of switching transitions between the two carriers is more pronounced (Fig. 3.6). Of special interest is the case with $\alpha = 0.5$ since it represents the most desirable operating point (upf input). A clear advantage in the semiconductor losses is observed with the sawtooth carrier for this case (Fig. 3.13(c)).



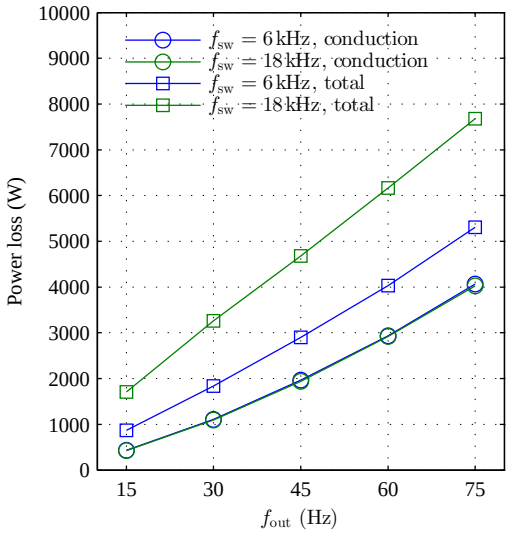
(a) $\alpha = 0$, triangular carrier

(b) $\alpha = 0$, sawtooth carrier

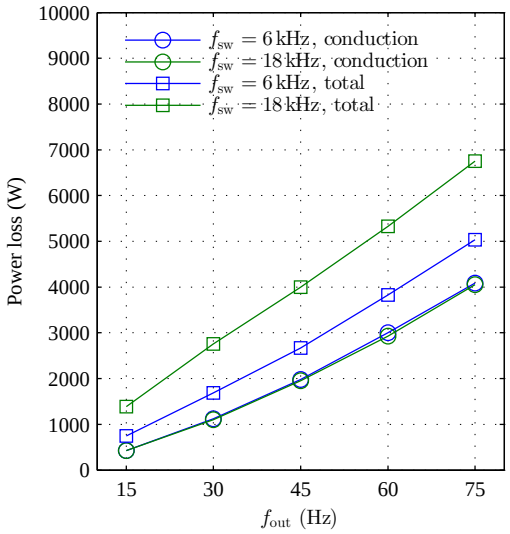
(c) $\alpha = 1$, triangular carrier

(d) $\alpha = 1$, sawtooth carrier

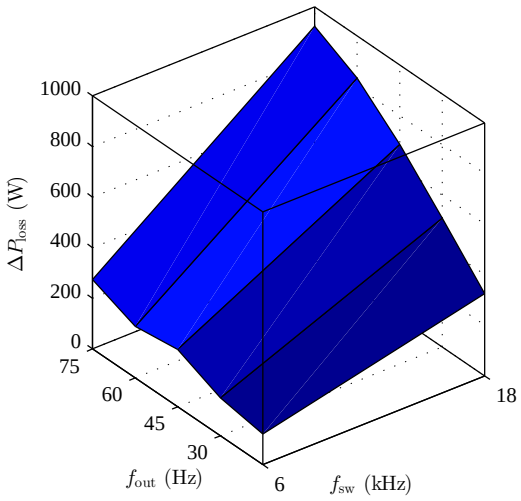
Figure 3.12: Semiconductor losses in the DMC based OE Wdg. drive at different operating points when modulated using only one set of vectors.



(a) $\alpha = 0.5$, triangular carrier



(b) $\alpha = 0.5$, sawtooth carrier



(c) Additional losses with a triangular carrier compared to sawtooth at $\alpha = 0.5$

Figure 3.13: Semiconductor losses in the DMC based OE Wdg. drive at different operating points when modulated for unity input power factor.

3.3 Simulation of the IMC OE Wdg. drives

This section presents the results of the simulation of the I-type and the T-type indirect matrix converter based open-end winding drives using the same loss calculation framework and the same operating points as the last section. The effect of the carrier will be discussed within the subsections discussing the waveform quality and the losses. Semiconductor devices and input filter identical to the previous section are used.

3.3.1 Waveform quality

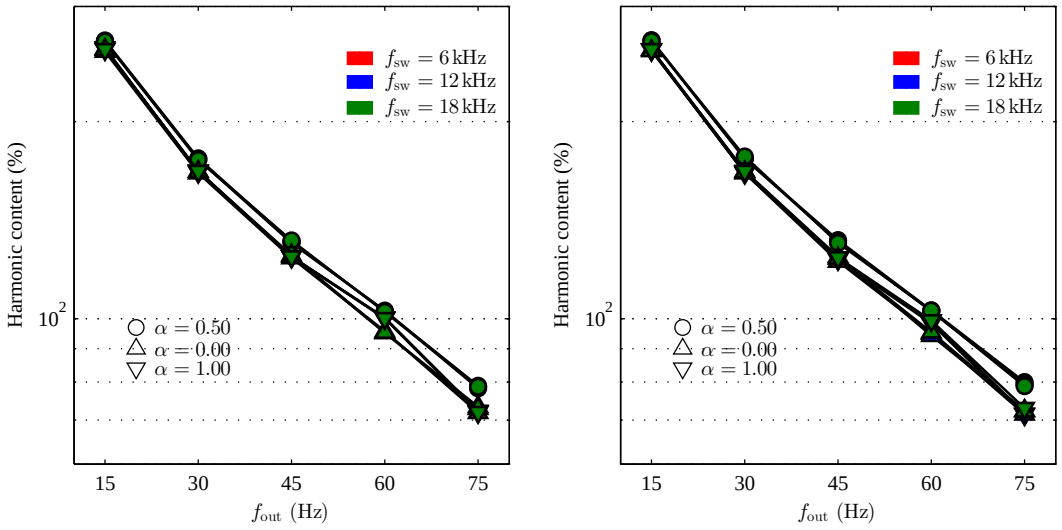
The harmonic content in the output voltage (Fig. 3.14) and the input current (Fig. 3.15) across all operating points for different carriers are shown for both of the indirect topologies, where the harmonic content is defined in (3.7).

As found in the direct matrix converter case, the harmonic content in the output voltage is independent of the switching frequency and the carrier used. A reduction in the harmonic content of the input current with higher switching frequency is also observed. The harmonic content in the input current also seems somewhat lower with the triangular carrier at most, but not all, operating points.

3.3.2 Power factor control

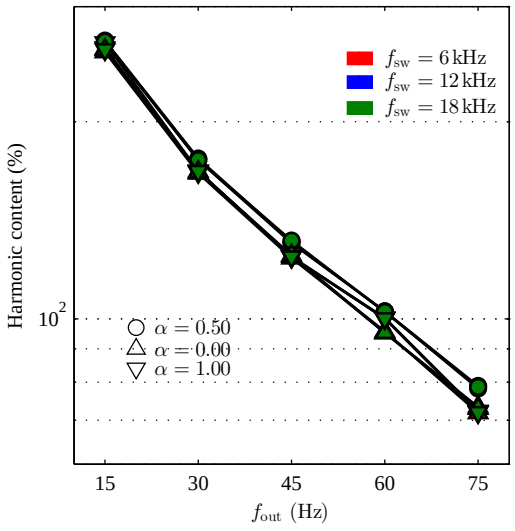
The plots of the power factor angle for all operating points are shown in Fig. 3.16(a) for the I-type topology and in Fig. 3.16(c) for the T-type topology. The results are similar to the previous section on the DMC based OE Wdg. drive since the converter topology does not affect the fundamental frequency behavior.

The power factor control ranges for both of the indirect topologies are illustrated in Figs. 3.16(b) and 3.16(d), and they are similar to the power factor range of Fig. 3.11(b) for the direct MC OE Wdg. drive.

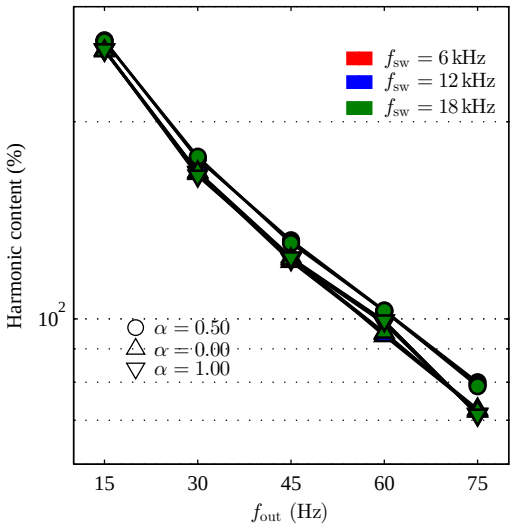


(a) I-type, triangular carrier

(b) I-type, sawtooth carrier

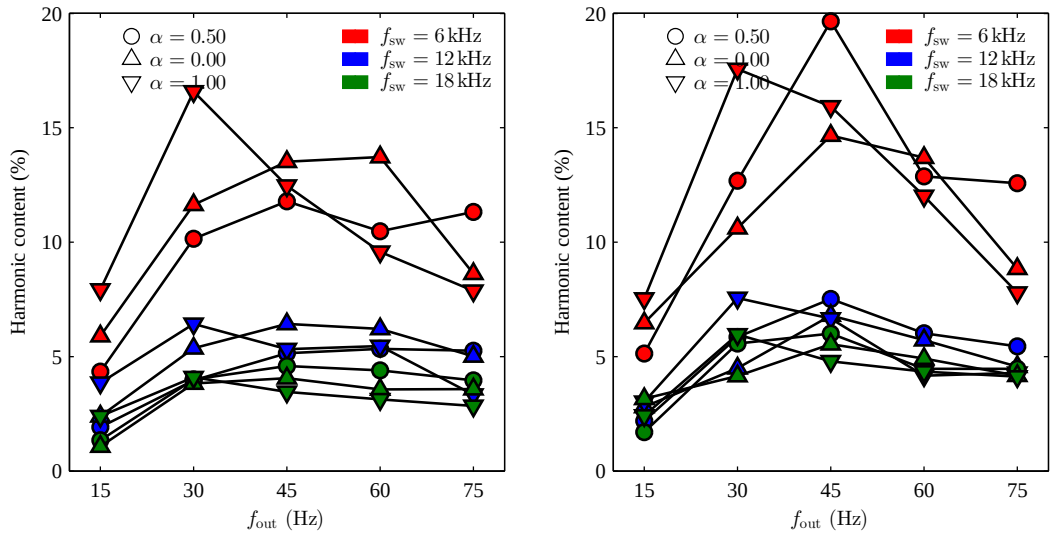


(c) T-type, triangular carrier



(d) T-type, sawtooth carrier

Figure 3.14: Harmonic content in the output voltage.



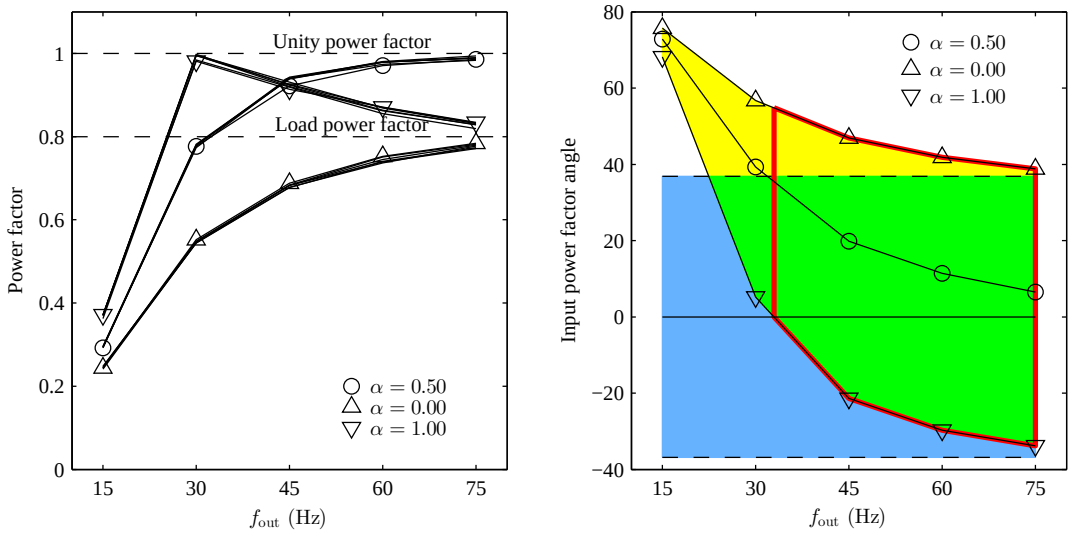
(a) I-type, triangular carrier

(b) I-type, sawtooth carrier

(c) T-type, triangular carrier

(d) T-type, sawtooth carrier

Figure 3.15: Harmonic content in the input current.



(a) Input power factor at all operating points (I-type)

(b) Input power factor control range with filter capacitors (I-type)

(c) Input power factor at all operating points (T-type)

(d) Input power factor control range with filter capacitors (T-type)

Figure 3.16: Input power factor control.

3.3.3 Semiconductor losses

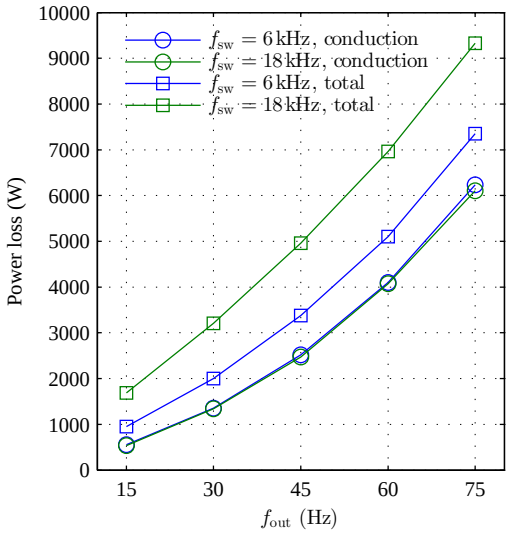
It is desirable that an electric drive draws sinusoidal currents in phase with the input voltages. Even though the cases $\alpha = 0, 1$ have been considered earlier for completeness, in general a matrix converter based open-end winding drive would operate at $\alpha \gtrapprox 0.5$ (α needs to be slightly higher than 0.5 to compensate for the leading current drawn by the input filter).

The semiconductor losses in the I-type indirect drive for $\alpha = 0.5$ are shown in Fig. 3.17, and Fig. 3.18 shows the semiconductor losses at the same conditions for the T-type drive. Losses have been computed for both carriers. As observed in the case of the direct matrix converter based drive, the conduction losses are unaffected by the choice of the carrier and the switching frequency; and the switching losses increase with the switching frequency. An advantage in the semiconductor losses is observed with the sawtooth carrier for both of the indirect drives (Figs. 3.17(c), 3.18(c)).

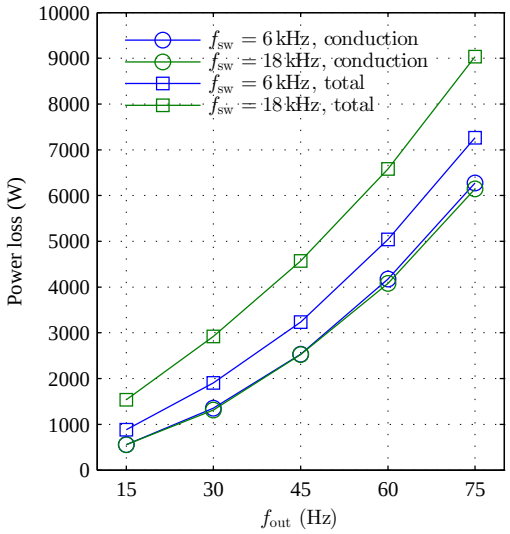
Validation of the proposed loss-optimal vector sequence

In the last chapter, two vector sequences that minimized the number of transitions in the load-end converters were identified. Between the two sequences identified, one sequence had the additional property of distributing the switching transitions among the phase legs more symmetrically and eliminating the $v_{\max} \leftrightarrow v_{\min}$ transitions. Therefore further reduction in the switching losses due to overall reduction in the voltage switched was expected.

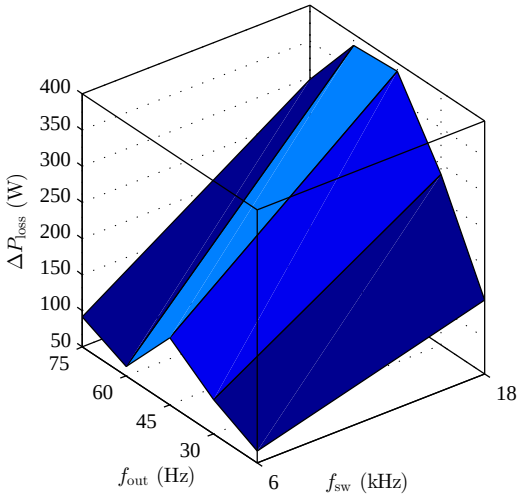
The dependence of the losses on the vector sequence is investigated in Fig. 3.20 at the operating point $f_{\text{out}} = 60\,\text{Hz}, f_{\text{sw}} = 12\,\text{kHz}, \alpha = 0.50$ for the T-type topology with a triangular carrier. Results include the vector sequence without any rearrangement and the two sequences with minimum transitions. The two sequences with minimum transitions are also illustrated in Fig. 3.19. Following observations are made:



(a) $\alpha = 0.5$, triangular carrier

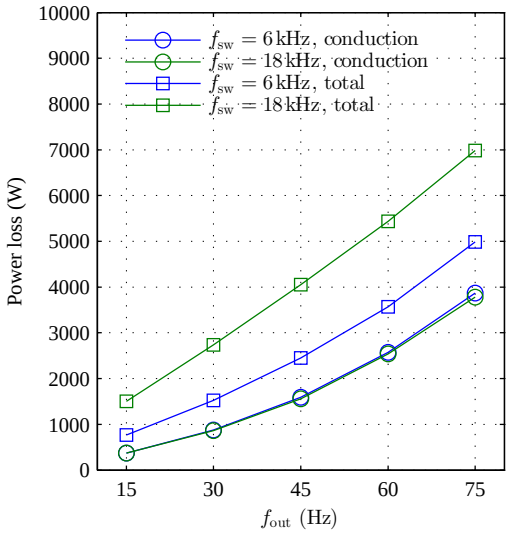


(b) $\alpha = 0.5$, sawtooth carrier

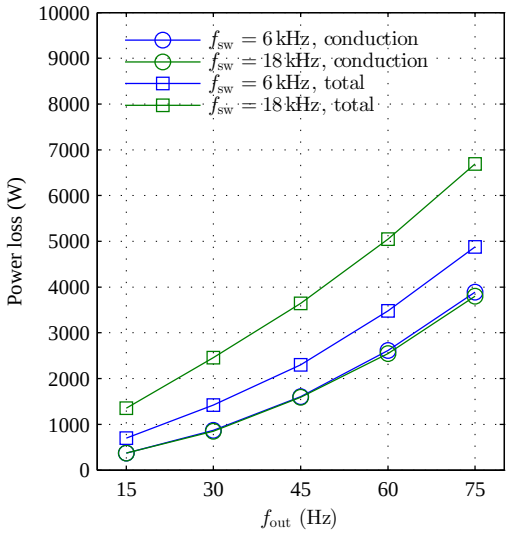


(c) Additional losses with a triangular carrier compared to sawtooth at $\alpha = 0.5$

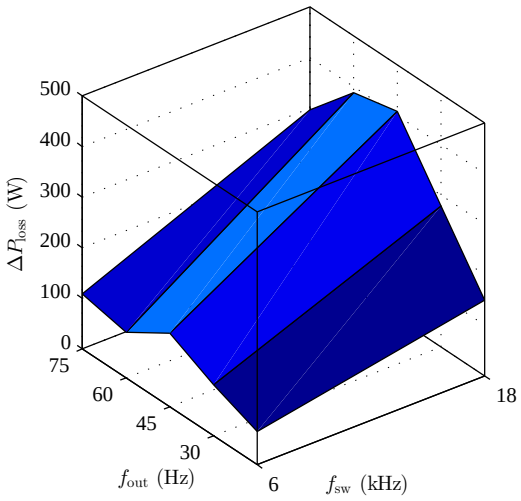
Figure 3.17: Semiconductor losses in the I-type indirect MC based OE Wdg. drive at different operating points when modulated for unity input power factor.



(a) $\alpha = 0.5$, triangular carrier

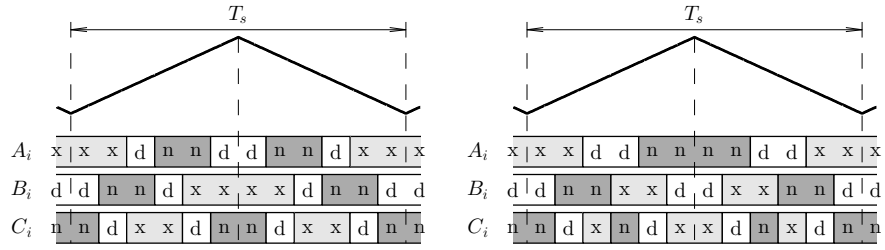


(b) $\alpha = 0.5$, sawtooth carrier



(c) Additional losses with a triangular carrier compared to sawtooth at $\alpha = 0.5$

Figure 3.18: Semiconductor losses in the T-type indirect MC based OE Wdg. drive at different operating points when modulated for unity input power factor.



(a) Vector sequence with the elimination of $v_{\max} \leftrightarrow v_{\min}$ transitions

(b) Vector sequence without the elimination of $v_{\max} \leftrightarrow v_{\min}$ transitions

Figure 3.19: Vector sequences with the minimum number of switching transitions.

- The conduction losses do not depend upon the vector sequence (expected),
- reducing the number of transitions reduces the switching losses (expected),
- and using the vector sequence of Fig. 3.19(a) that eliminates $v_{\max} \leftrightarrow v_{\min}$ transitions (middle plot in Fig. 3.20) reduces the switching losses further.

Although the validation of the proposed loss-optimal vector sequence is provided for only one topology at only one operating point, it is expected that the applicability would hold over all operating points and all topologies. The semiconductor losses discussed so

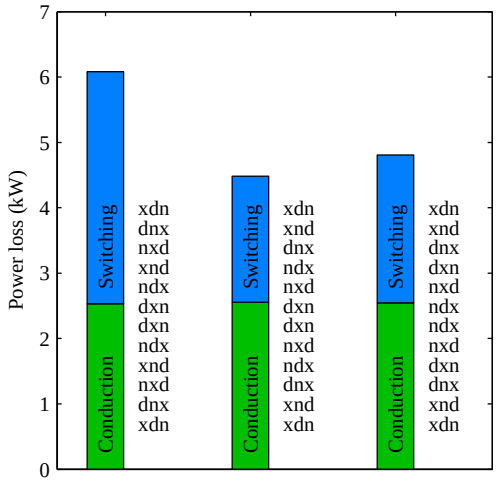


Figure 3.20: Vector sequences and semiconductor losses: without any rearrangement (left), minimum transitions with $v_{\max} \leftrightarrow v_{\min}$ elimination (middle, Fig. 3.19(a)), and minimum transitions without $v_{\max} \leftrightarrow v_{\min}$ elimination (right, Fig. 3.19(b)).

far in this chapter (with the exception of Fig. 3.20), use the proposed vector sequence (with $v_{\max}, v_{\text{mid}}, v_{\min}$ replaced by v_a, v_b, v_c respectively for the DMC OE Wdg. drive).

3.4 Summary and conclusions

3.4.1 Choice of the carrier

The output voltage harmonic content is found to be independent of the choice of the carrier for all three topologies. Slight reduction in the input current harmonic content with a triangular carrier is seen in all three topologies. However, the reduction is not present across all operating points and the relationship of the harmonic content with the carrier cannot be considered definite.

As argued earlier, even though the operating points with $\alpha = 0, 1$ are included for completeness, $\alpha = 0.5$ represents the most relevant operating points since operation at upf input conditions is almost always desired in drive applications. Comparing the semiconductor losses with the two carriers in Figs. 3.13(c), 3.17(c), and 3.18(c), it is seen that a sawtooth carrier performs better than a triangular carrier across all topologies. This is also consistent with the arguments made in the favor of the sawtooth carrier in Section 3.2.2 citing the lower number of switching transitions with the sawtooth carrier (Fig. 3.6).

Therefore, with possibly a slight disadvantage in the input current harmonic content and a clear advantage in the switching losses, a sawtooth carrier would be the carrier of choice for matrix converter based open-end winding drives.

3.4.2 Quality of the input and the output waveforms

A comparison of the output voltage harmonic content shown in Figs. 3.9(b) (direct MC, sawtooth), 3.14(b) (I-type, sawtooth) and 3.14(d) (T-type, sawtooth) shows that the harmonic content in the output voltage is similar for all three topologies. The simulations were run with ideal switches and ideal switching signals. In practice, the load terminals in the direct matrix converter based open-end winding drive will occasionally see the clamp voltage, increasing the output voltage distortion slightly.

A comparison of the input current harmonic content in Figs. 3.10(b) (direct MC,

sawtooth), 3.15(b) (I-type, sawtooth) and 3.15(d) (T-type, sawtooth) favors the direct matrix converter based open-end winding slightly over its indirect counterparts. No difference is noted between the two indirect implementations.

While not absolutely essential, in the direct matrix converter based open-end winding drive reported by Gupta, a third clamp circuit is connected at the input terminals to set the clamp capacitor voltage. The small current drawn by the clamp circuit will contribute toward additional harmonic content in the input current. Harmonic content in the input/output waveforms of the indirect implementations will, of course, remain unaffected by any clamp-related effects.

3.4.3 Components required

Table 3.2 shows the semiconductor, passive components, and the instrumentation requirements of the three matrix converter based open-end winding drives. All semiconductors are rated for 1200 V, 200 A (for the system considered). The input filter components are also identical for all three implementations.

The purpose of the clamp/brake IGBT and resistor was discussed earlier — this arrangement is necessary to stop the motor and prevent overvoltages in case of faults; and also to regulate the clamp capacitor voltage while avoiding static losses in the case of the direct implementation. A DC voltage sensor is necessary to monitor the clamp capacitor voltage or the voltage $v_{\max} - v_{\min}$ to trigger the brake IGBT.

Two AC voltage sensors are required to sense the balanced input voltages for modulation. Imbalance at the input may necessitate the use of third sensor.

The direct matrix converter based drive requires current sensing for intelligent commutation. While current sensing is not required for intelligent commutation in the indirect drives, AC current sensors are required for closed-loop operation (discussed in the next chapter). Only two AC current sensors are required for motor currents; a third sensor, however, may be included to sense the low-frequency common-mode current.

The circuit protection components (fuses, relays etc.) are not included in Table 3.2. The protection requirements are expected to be identical.

Overall, the I-type indirect matrix converter based open-end winding drive has the highest semiconductor requirements although the addition of a third clamp circuit would

Component	DMC	I-type	T-type	
IGBTs with free-wheeling diodes	36	36	36	
Clamp/NPC diodes	12	18	–	Semiconductors
Clamp capacitor discharge/brake IGBT	1	1	1	
Filter (L_f, C_f, L_d, r_d)	Identical	Identical	Identical	
Clamp capacitor	1	–	–	Passives
Clamp capacitor discharge/brake resistor	1	1	1	
AC voltage sensors	2 (3)	2 (3)	2 (3)	
AC current sensors	2 (3)	2 (3)	2 (3)	Instrumentation
DC voltage sensor	1	1	1	

Table 3.2: Semiconductor, passive component, and instrumentation requirements of the three matrix converter based open-end winding drives.

bring the semiconductor requirements of the DMC OE Wdg. drive on par with the I-type. Due to the clamp capacitor, the direct drive has the highest passive component requirements even though the filters for all three implementations are identical. The instrumentation requirements for the three drives are identical. The T-type indirect drive has the lowest semiconductor and the lowest passive component requirements among all implementations.

3.4.4 Semiconductor losses

The semiconductor losses for the three topologies were discussed individually in the previous sections. Fig. 3.21 shows the conduction losses for the three topologies on the same plot for $\alpha = 0.5$: plots at all switching frequencies for both carriers are included although, as expected, the switching frequency and the carrier have no effect on the conduction losses.

At any given instant in the I-type drive, 18 semiconductor devices conduct; the number of conducting devices is 12 for the T-type and the direct drive. Consequently the conduction losses in the I-type drive are the highest among the three.

In the T-type drive, the input current corresponding to the input phase with the highest instantaneous voltage is conducted through only one IGBT (or only one diode)

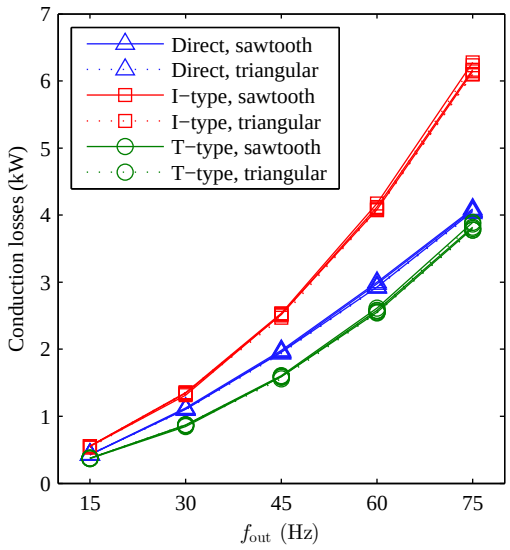


Figure 3.21: Conduction losses for the matrix converter based drives at $\alpha = 0.5$.

at near upf input conditions. The same holds true for the input current corresponding to the lowest instantaneous voltage. In the direct drive, all currents are conducted by two devices at all times. Therefore the conduction losses in the T-type drive are somewhat lower than the direct matrix converter based drive, even though the total number of conducting devices is the same. Overall, the T-type indirect matrix converter drive incurs the lowest conduction losses.

The switching losses for the three topologies at $f_{\text{sw}} = 18\,\text{kHz}$ and $\alpha = 0.5$ are shown in Fig. 3.22. We have already established that using a sawtooth carrier results in lower switching losses, and it is observed once again in Fig. 3.22. The switching losses of the two indirect implementations are identical as expected. At higher loads, the direct matrix converter based drive shows a slight advantage in the switching losses (with the recommended sawtooth carrier). However, the slight advantage is not enough to offset the higher conduction losses as seen in Fig. 3.23, that shows the total losses at $f_{\text{sw}} = 18\,\text{kHz}$.

The total losses are the lowest for the T-type drive, followed by the direct matrix converter based drive. Due to the high conduction losses, the total losses are the highest for the I-type drive. Although the Fig. 3.23 is at $f_{\text{sw}} = 18\,\text{kHz}$, the T-type drive will

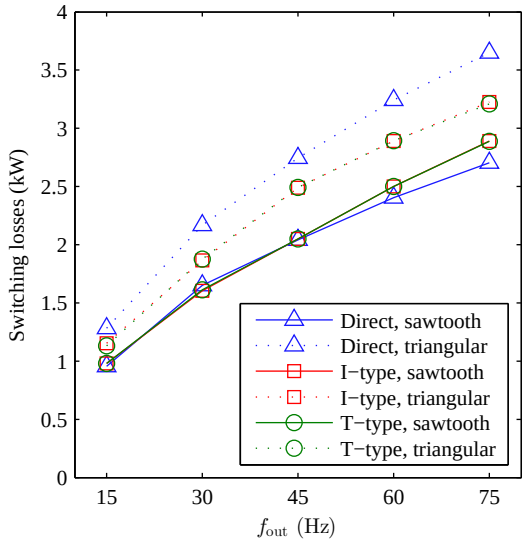


Figure 3.22: Switching losses for the matrix converter based drives at $\alpha = 0.5$.

have the lowest losses at $f_{sw} < 18\,\text{kHz}$ as well since its conduction losses are the lowest (Fig. 3.21). It is, however, possible that the direct matrix converter based drive could have lower losses than the T-type drive at switching frequencies higher than 18 kHz.

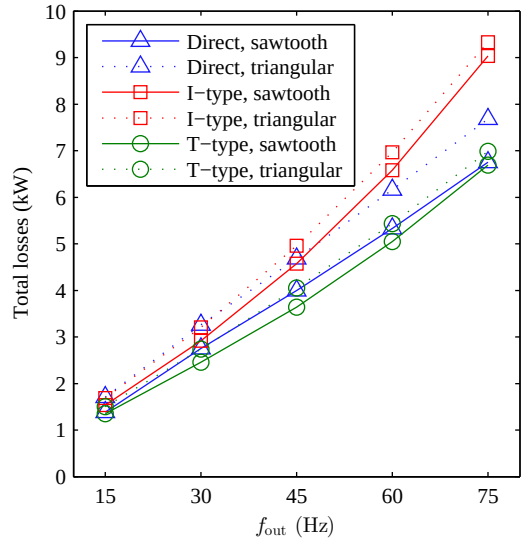


Figure 3.23: Total losses for the matrix converter based drives at $\alpha = 0.5$.

Sources of error

The model used for loss calculation is data-driven, and it does not model the physical processes of semiconductor conduction and switching. Further inaccuracies are caused due to limited data and simplistic thermal modeling. Some disagreement with the manufacturer's loss estimation software also exists.

On occasion, the simulation software used predicts negative switching losses that are ignored (clipped at zero). While the absolute values of the individual data points ignored is insignificant compared to $E_{\mathrm{ON}}, E_{\mathrm{OFF}}, E_{\mathrm{RR}}$, it is possible that the cumulative magnitude causes a significant error. A possible reason for the prediction of negative losses may be the incorrect assignment of the device in which losses are incurred.

Therefore a certain degree of error is to be expected in the values estimated. Based on the disagreement with the manufacturer's software for the loss estimation of simple circuits, the error seems to be in the range of 10%–20%. The accuracy of the manufacturer's software is itself not published. A complete evaluation of the conclusions related to the semiconductor losses is possible only by measurements made on experimental prototypes at the rated values which is beyond the scope of this work.

3.4.5 Conclusions

Based on the results and the discussion in this section, a sawtooth carrier is recommended for matrix converter based open-end winding drives due to its lower losses and similar harmonic distortion as the triangular carrier.

The harmonic distortion in the output voltages of all three matrix converter based open-end winding drives is similar. The input current distortion is somewhat better in the direct matrix converter drive. However, inclusion of the necessary clamp circuits is expected to degrade the output voltage distortion and possibly the input current distortion to some degree in a practical circuit. Therefore, the waveform quality with all three topologies will likely be similar.

The effect of the filter capacitor on the input power factor is, as expected, same for all three topologies.

Based on its higher semiconductor count and high semiconductor losses, the I-type indirect drive is excluded from further consideration. The T-type indirect drive uses

lesser semiconductor and passive components compared to the direct matrix converter based drive. The semiconductor losses are also lower. Furthermore, the advantages of the indirect approach include naturally intelligent commutation and natural LVRT integration. Some additional losses may occur in the direct matrix converter based drive due to the reverse recovery in the clamp diodes.

As a result of its lowest semiconductor and passive parts count, lowest semiconductor losses, and additional advantages of naturally intelligent commutation and the possibility of LVRT implementation without additional components, the T-type drive of Figs. 1.9(b) and 2.12(b) emerges as the most promising topology among the three matrix converter based open-end winding drives. In the next chapter, this T-type drive will be compared against the state-of-the-art drive systems using a closed-loop motor control framework.

Chapter 4

Matrix converter based open-end winding drives: a comparison with the state-of-the-art

The theory of operation of matrix converter based open-end winding drives for common-mode voltage elimination was discussed in Chapter 2. Experimental results were provided to prove the drives operation. The analysis of the common-mode performance was reserved for later. In this chapter, experimental evidence of common-mode voltage elimination in the indirect matrix converter based open-end winding drives will be provided. Results showing significant reduction in the shaft voltage and the ground current compared to the state-of-the-art will prove the superior common-mode performance of the presented drives. A related issue of circulating currents in the open-end winding drives, and possible solutions to this issue will also be discussed.

Having established the common-mode reduction in the presented drives experimentally, these drives will be compared against the state-of-the-art converters on the input/output waveform quality, semiconductor and passive parts count, and semiconductor losses, to determine if the matrix converter based open-end winding drives present a viable alternative. The analysis will be conducted for a typical industrial motor drive. The T-type indirect topology will be used as the representative of the matrix converter based open-end winding drives due to its advantages over the other two implementations

(direct and I-type indirect).

4.1 Common-mode performance of the presented drives

The introduction to this dissertation briefly discussed the generation of the common-mode voltage in the state-of-the-art drives. These drives use a voltage source inverter (VSI) to generate variable frequency AC output voltages from one or more DC input voltages. Two- and three-level inverters (2L-VSI, 3L-VSI) are common in industrial drives although medium- and high-voltage applications favor multilevel [38] and modular multilevel inverters [81–88].

Chapters 2 and 3 discussed three topologies of matrix converter based open-end winding drives for common-mode elimination. In this section the common-mode performance of the presented indirect matrix converter based open-end winding (IMC OE Wdg.) drives will be evaluated against the VSIs used in the state-of-the-art systems. The I-type IMC OE Wdg. drive will be used for the common-mode comparison. Results from the T-type IMC OE Wdg. drive are expected to be similar.

Common-mode voltages at the motor terminals excite the motor parasitic capacitances and cause ground currents (from the motor terminals, into the earth ground). These ground currents cause electromagnetic interference. The detrimental bearing currents are also a part of the ground currents. Shaft voltage can be used an indicator of the bearing currents [7, 8]. Therefore, measuring ground currents and shaft voltages provides an estimate of the undesirable effects of the output common-mode voltage.

Fig. 4.1 shows the AC induction motor of Table 2.13 fitted with a brush and a grounding braid to measure the shaft voltage and the ground current. An off-the-shelf shaft-grounding brush is mounted such that the brush is in electrical contact with the motor shaft but the housing (connected electrically to the brush) is isolated from the motor body. A grounding braid connects the motor assembly to the earth ground. No other path to the earth exists and the entire ground current must flow through the grounding braid. A small cable is inserted to enable the current measurement using a high-bandwidth current probe. A Rogowski current probe (bandwidth 1 MHz) is also connected to measure any low-frequency common-mode current flowing in the stator windings.

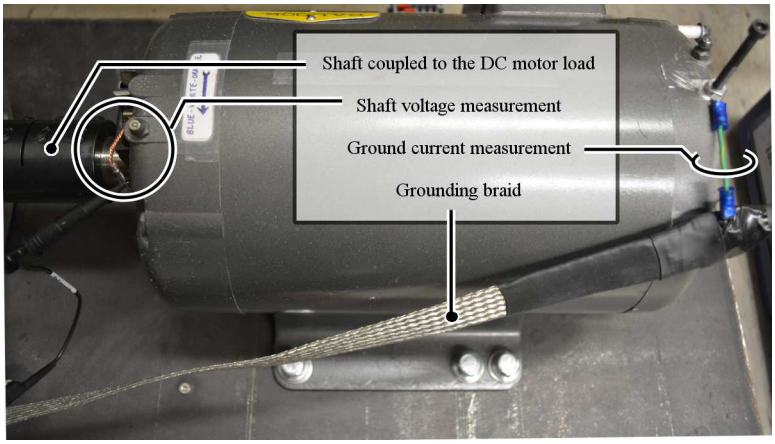
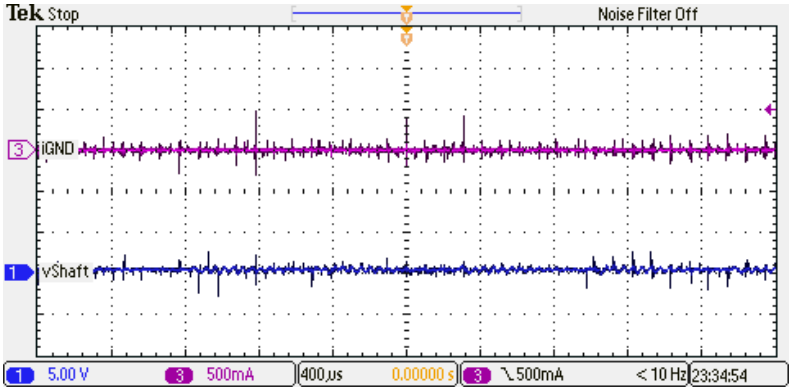


Figure 4.1: Setup for the measurement of shaft voltage and ground current.

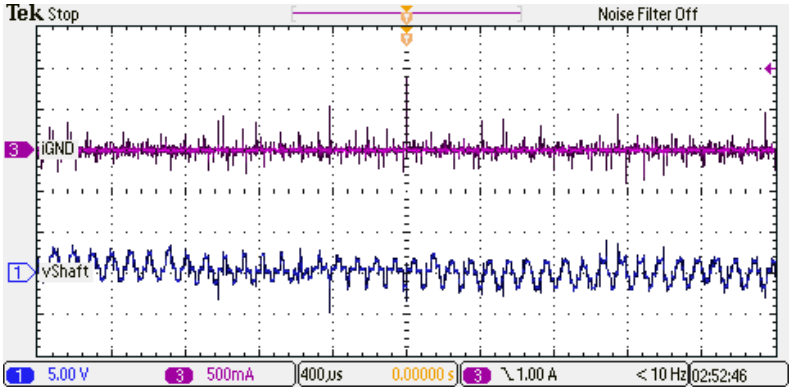
To evaluate the common-mode performance of different drive topologies, the motor was driven from each of the following drives: I-type indirect matrix converter based open-end winding drive (I-type IMC OE Wdg.), two-level VSI (2L-VSI), and three-level VSI (3L-VSI). The circuit of the matrix converter based drive has already been described in a previous chapter. To realize the 2L-VSI, a part of the T-type topology (circuit diagram in Fig. 2.12(b)) was controlled using symmetrical space vector pulse width modulation [2]. The 3L-VSI was realized using one three-phase three-level bridge of the I-type topology (circuit diagram in Fig. 2.12(a)) and was controlled using sine-triangle PWM with third harmonic injection [2]. Regulated DC voltage sources were used for both the VSIs.

An input voltage of $\approx 135\,\mathrm{V}$ was used for the matrix converter based open-end winding drive. At this input voltage and at its maximum voltage transfer ratio, the drive generates the rated motor voltage. The DC bus voltage for the VSIs was $\approx 290\,\mathrm{V}$ (split between two $\approx 145\,\mathrm{V}$ buses for the 3L-VSI). The inverters generate the rated motor voltage at full modulation index for this DC input. The output voltage is set according to $V/f = 200/60\,\mathrm{V/Hz}$ and the output fundamental frequency f_{out}. The switching frequency f_{sw} is $\approx 10\,\mathrm{kHz}$ in all cases.

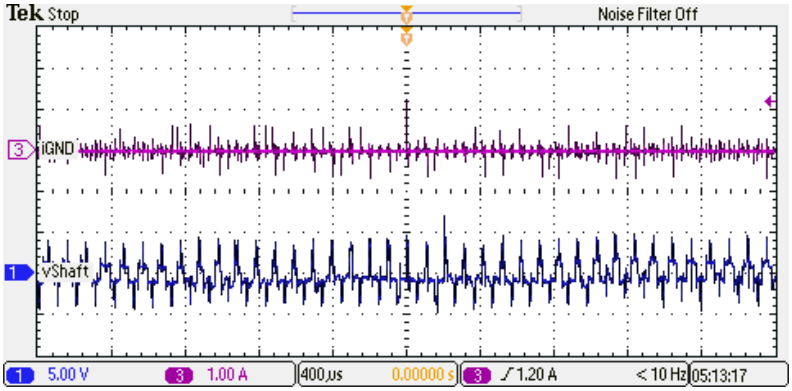
Fig. 4.2 shows the shaft voltage and the ground current for the I-type IMC OE Wdg. drive and the two VSI based state-of-the-art drives. Consistent with the literature, the common-mode effects are lower in the 3L-VSI as compared to the 2L-VSI. However,



(a) I-type indirect matrix converter based open-end winding (I-type IMC OE Wdg.) drive



(b) Three-level VSI (3L-VSI)



(c) Two-level VSI (2L-VSI)

Figure 4.2: Shaft voltage and ground current for (a) the I-type IMC OE Wdg. drive, (b) 3L-VSI and (c) 2L-VSI. Note that the top two plots use 500 mA/div whereas the bottom plot uses 1 A/div scaling for the ground current. $f_{\text{out}} = 50\,\text{Hz}$.

the shaft voltage and the ground current, both, are lowest in the presented IMC OE Wdg. drive (Fig. 4.2(a)). Very few current spikes with a magnitude larger than 200 mA are observed in the presented drive whereas such spikes are more frequent, and have a higher magnitude, with the VSIs. No definite shape of the near-zero shaft voltage is noted in the matrix converter drive as opposed to the VSIs where the shaft voltage follows the shape of the common-mode voltage generated.

The output frequency in Fig. 4.2 is 50 Hz. Similar results (relatively smaller and infrequent spikes in ground currents, near-zero shaft voltage) are observed at other operating conditions and time scales. Table 4.1 compares the rms and the peak values of the ground currents for the three drives at several different operating points. A clear reduction in the ground currents is observed with the IMC OE Wdg. drive. Coupled with the near-zero shaft voltage (Fig. 4.2(a)), it is expected that the bearing currents in the matrix converter based open-end winding drives would be extremely small.

However, as small as the ground currents are, they are not zero. The presence of finite ground currents is due to the finite common-mode voltage present in the drive output — during the dead time included for safe commutation, the voltages at the machine terminals do not add to zero. This is illustrated in Fig. 4.3 for the single-ended version of the I-type indirect matrix converter based drive (Fig. 2.1). The vector applied at the machine terminal switches from $\vec{v}_{\text{xnd}}$ to $\vec{v}_{\text{dxn}}$. During the commutation, two load phases get connected to the same link voltage resulting in a net common-mode voltage.

Therefore, presence of finite dead time is a source of common-mode voltage generation in the MC-based OE Wdg. drives. Yet another source of common-mode voltage generation is the finite voltage drop across the conducting devices. These sources of

	peak (mA)			rms (mA)		
f_{out} (Hz)	IMC OE Wdg.	3L-VSI	2L-VSI	IMC OE Wdg.	3L-VSI	2L-VSI
30	520	760	1360	26	46	83
40	500	960	1360	26	49	84
50	480	920	1400	26	48	85
60	580	960	1320	25	48	86

Table 4.1: Comparison of rms and peak values of ground currents in different drive topologies.

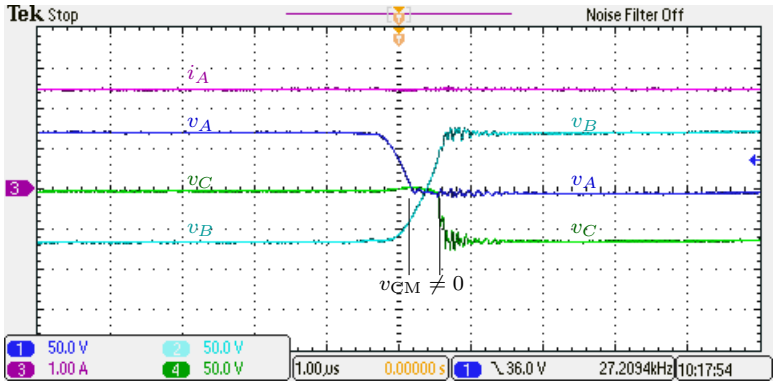


Figure 4.3: Common-mode voltage generation during commutation.

common-mode voltage generation have been discussed in [64, 79] for the direct matrix converter based open-end winding drive. The dead time and the device drops lead to high-frequency as well as low-frequency common-mode voltage generation. A difference between the common-mode voltages at the two sets of machine terminals, coupled with the low common-mode impedance offered by the stator windings ($R_s + L_{ls}$ per phase) at low frequencies, results in rather large 'circulating currents' — circulating currents are low-frequency common-mode currents that flow from one machine terminal to the other as opposed to the high-frequency common-mode currents that flow from both sets of the machine terminals into the earth ground.

The presence of low-frequency common-mode currents (circulating currents) is noted in Fig. 4.4. Even though the ground currents are lower in the presented drives, the rms value of the common-mode currents is *higher* than the VSI based drives due to the circulating currents as shown in Table 4.2. While benign in comparison to the high-frequency common-mode currents, the low-frequency circulating currents are still undesirable due to the ohmic losses caused. Furthermore, these currents may render ineffective any common-mode impedance added to attenuate the high-frequency common-mode currents.

The solutions used to impede the common-mode current in VSIs are also applicable here. Gupta and Somani [64, 79] have discussed the passive approach of adding a common-mode choke as well as the active approach of modifying the commutation

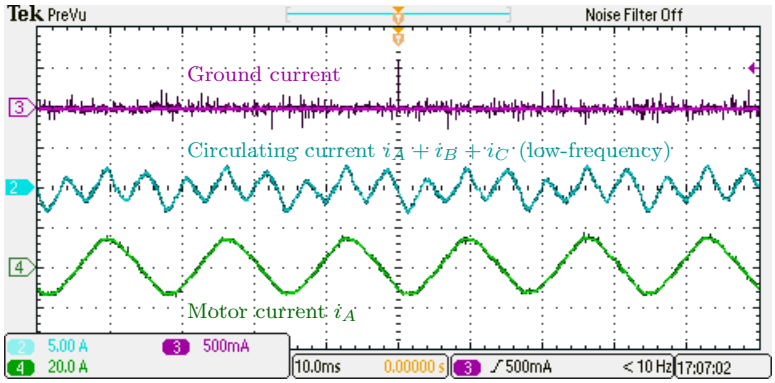


Figure 4.4: Circulating current in the I-type indirect matrix converter based open-end winding drive. $f_{\text{out}} = 60\,\text{Hz}$.

pattern. The active approach has been investigated further by Baranwal [89]. A zero-sequence current controller [90] may prove highly effective in eliminating the circulating currents without having to add common-mode impedance.

Based on the results from the I-type IMC OE Wdg. drive, it is concluded that matrix converter based open-end winding drives significantly reduce the shaft voltage and the ground currents. In particular, the near-zero values of the shaft voltage suggest nearly complete elimination of the bearing currents. However, the finite switching times and the finite device drops do not allow a complete elimination of the common-mode voltage and thus the ground currents. Moreover, the difference in the common-mode voltages at the two sets of terminals results in large circulating currents.

	IMC OE Wdg.		3L-VSI		2L-VSI	
f_{out} (Hz)	i_A (A)	i_{CM} (A)	i_A (A)	i_{CM} (A)	i_A (A)	i_{CM} (A)
30	6.42	0.41	6.43	0.0115	6.32	0.0275
40	7.35	0.39	7.26	0.0125	7.24	0.0278
50	8.36	0.45	8.18	0.0126	8.18	0.0281
60	9.35	0.46	8.98	0.0124	9.38	0.0285

Table 4.2: Comparison of the low-frequency common-mode current (rms) for different drive topologies: i_{CM} is measured using a 1 MHz probe and some high-frequency components are attenuated. The rms value of the phase current is included for reference.

4.2 A framework for comparison against state-of-the-art

In the previous section, the superior common-mode performance of the matrix converter based open-end winding drives was demonstrated using the I-type IMC OE Wdg. drive. Small values of shaft voltage suggested a nearly complete elimination of the bearing currents; overall reduction in the ground currents was also observed.

In this section, a framework for comparing the matrix converter based open-end winding drives to the back-to-back VSI based drives will be established such that the semiconductor losses, semiconductor and passive parts count, and input/output waveform quality can be compared under uniform conditions for a typical industrial drive. The conclusions related to the common-mode performance drawn in the previous section would be assumed to extend to larger motors as well.

4.2.1 Back-to-back VSIs

Voltage source inverters fed from regulated DC voltage sources were used for comparison in the previous section. In a practical drive system, the DC voltage is generated from the input AC voltages using a rectifier. VSIs identical to the ones that drive the motor can also be used in place of a traditional diode rectifier for better input current quality and bidirectional power flow among other advantages. Back-to-back converters, where the front-end (grid-side) and the load-end converters are both VSIs, are treated as the state-of-the-art in this dissertation. A two-level inverter is the simplest voltage source inverter and several leading manufacturers use this inverter topology. The block diagram of the two-level back-to-back converter (2L-BBC) based drive is shown in Fig. 4.5. The grid-side VSI (front-end) generates a regulated DC voltage. It is also responsible for the input power factor control. The inductors connected at the front-end input

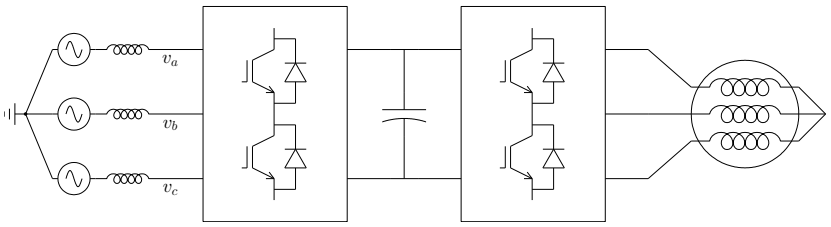


Figure 4.5: Two-level back-to-back converter (2L-BBC) based drive.

provide grid current filtering. Instead of a first-order inductive filter, higher order filters (e.g. $LCL, LLCL$) may be used to reduce the cost and the size of the input inductor [12, 77, 91, 92].

The three-level-neutral-point-clamped (NPC) inverter, proposed by Nabae *et al.* in 1981 [93], has a lower output harmonic distortion as compared to a 2L-VSI. The output common-mode characteristics are also better as shown in the previous section. The 2L-VSIs in Fig. 4.5 can be replaced by 3L-VSIs to arrive at the three-level back-to-back converter (3L-BBC) based drive shown in Fig. 4.6. The principle of operation is similar to the 2L-BBC: the front-end generates a split DC bus and the load-side VSI connects each one of the motor terminals to the three DC levels alternately.

The matrix converter based open-end winding drives will be compared to both back-to-back converter topologies, two-level and three-level, in this chapter.

4.2.2 Semiconductor devices used for comparison

Since the aim of this analysis is to compare the different drives at a typical industrial power/voltage level, most of the conclusions will be drawn using simulations. The base system used in the previous chapter will be used again (480 V, 80 kVA). The amplitude of the line-to-line voltage for this system is 678.8 V. This is also the minimum DC bus voltage necessary for the VSIs to be able to generate the base voltage at the input and the output. In practice, a somewhat higher voltage is necessary to compensate for the voltage drop across the input inductors. Therefore the DC bus voltage is chosen to be 800 V.

The semiconductor devices of the 2L-BBC of Fig. 4.5 need to block this DC bus voltage whereas the semiconductor devices of the 3L-BBC of Fig. 4.6 need to block half

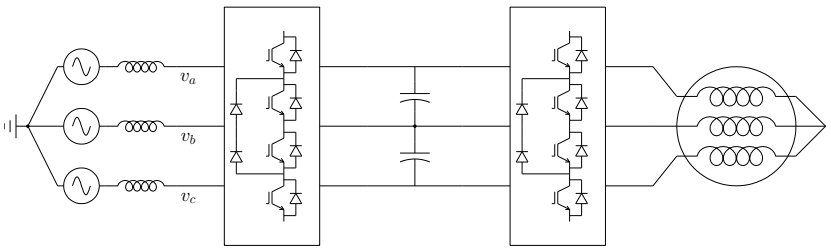


Figure 4.6: Three-level back-to-back converter (3L-BBC) based drive.

of this voltage. Leaving a 33% margin of safety, the IGBT module CM200DU-24NFH, used in the previous chapter for matrix converters, is found suitable for the 2L-BBC as well. For the 3L-BBC, a 600 V, 200 A IGBT from the same product family, CM200DU-12NFH, will be used. The semiconductor loss calculation model for the former IGBT has already been discussed. A semiconductor loss calculation model was constructed for the latter IGBT using the same assumptions. The losses predicted by the model show good agreement with the manufacturer's loss estimation software (Table 4.3).

4.2.3 Motor, control, and operating points used

A 460 V, 75 hp motor is chosen for comparing the matrix converter based open-end winding drive against the back-to-back VSI based drives on the criteria of waveform quality, semiconductor losses, and parts count. The equivalent circuit parameters of

	IGBT switching (W)		IGBT conduction (W)	
	Manufacturer's software	Simulated	Manufacturer's software	Simulated
OP1	45	45	74	85
OP2	66	66	191	202
OP3	33	33	191	204
OP4	36	37	15	20
	Diode switching (W)		Diode conduction (W)	
	Manufacturer's software	Simulated	Manufacturer's software	Simulated
OP1	20	20	68	78
OP2	28	28	60	67
OP3	14	14	60	67
OP4	17	18	39	48
	IGBT T_j(°C)		Diode T_j(°C)	
	Manufacturer's software	Simulated	Manufacturer's software	Simulated
OP1	50	52	51	46
OP2	76	82	56	45
OP3	69	74	51	42
OP4	36	37	41	39

Table 4.3: Comparison of the losses calculated in the simulation against the manufacturer's software for IGBT CM200DU-12NFH.

this motor are provided in Table 4.4. This motor is controlled using the indirect rotor field-oriented control [94]. In simulations a lower moment of inertia is used to accelerate the steady state.

The analysis is conducted at a total of six operating points ranging from fully-motoring to fully-generating, and including no-load and standstill conditions. These operating points are marked on the torque-speed plane in Fig. 4.7. The analysis is conducted at three switching frequencies $f_{\text{sw}} = 6\,\text{kHz}, 12\,\text{kHz}, 18\,\text{kHz}$. For all drive systems, unity input power factor is used — this is accomplished by closed-loop control in the VSI based drives and by using suitable value of the power factor control parameter α in the matrix converter drive. The T-type indirect matrix converter based open-end winding drive topology is chosen as the representative topology among the three matrix converter drives due to its lower parts count and lower semiconductor losses compared to the other two implementations (I-type indirect and direct matrix converter based).

Parameter	Value
Rated voltage	$460\,\text{V}, 60\,\text{Hz}$
Number of poles, p	4
Stator resistance, R_s	$0.0580\,\Omega$
Stator leakage inductance, L_{ls}	$0.5333\,\text{mH}$
Magnetizing inductance, L_m	$23.1333\,\text{mH}$
Rotor resistance, R_r	$0.0667\,\Omega$
Rotor leakage inductance, L_{lr}	$0.5333\,\text{mH}$
Moment of inertia, J	$20\,\text{kg}\,\text{m}^2$

Table 4.4: Parameters of the motor used for comparison.

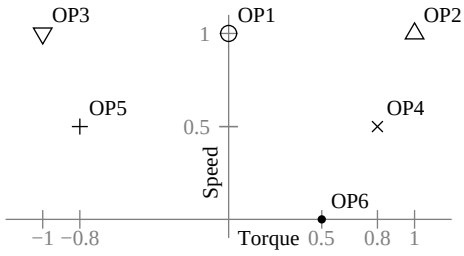


Figure 4.7: Operating points used for the analysis.

4.3 Back-to-back two-level VSI (2L-BBC) based drive

This section reviews the results from the simulation of the back-to-back two-level VSI (2L-BBC) based drive. The semiconductor losses are quantified for all operating points of Fig. 4.7. The harmonic content in the input current is calculated at all operating points except at the no-load and the standstill conditions (OP1, OP6 in Fig. 4.7); the harmonic content in the output currents is calculated at all operating points except at standstill (OP6 in Fig. 4.7).

Before discussing the losses and the harmonic distortion, the passive component requirements are evaluated and the values used in the simulations are provided. The semiconductor and the instrumentation requirements are discussed at the end of this chapter.

4.3.1 Passive components required in 2L-BBC drive

Input inductor

At the AC side, the front-end converter applies a pulse width modulated voltage that has a fundamental component *approximately* equal to the grid voltage — the equivalent circuit of the front-end converter at the fundamental frequency is two voltage sources connected through a reactance. The active and the reactive power flow is controlled by varying the magnitude and the phase angle of the front-end AC voltage with respect to the grid.

The switching frequency component of the front-end voltage causes a high-frequency current to flow through the input inductor. The peak-to-peak value of this high-frequency current depends upon the modulation index, the DC bus voltage, the switching frequency, and the input inductance. Let the modulation index be m, the DC bus voltage be V_{DC}, and the switching frequency be denoted as f_{sw} as before. Let the input inductor be L_f — same notation as the filter inductor in the matrix converter based drives is being used. It has been shown in the literature [95–97] that the peak-to-peak current ripple can be calculated as:

$$\tilde{i}_{\text{pp}} = \frac{mV_{DC}}{2\sqrt{3}L_f f_{\text{sw}}} \qquad m \in [m^*, 1/\sqrt{3}] \tag{4.1}$$

where $\tilde{i}_{\text{pp}}$ is the peak-to-peak ripple and $m^* = 2/3(1 - 1/\sqrt{3})$. The maximum value of the modulation index for two-level (and three-level) VSIs is $1/\sqrt{3}$. Inductance L_f can be chosen based on the specifications on the maximum current ripple and further evaluated in simulation for the total harmonic content in the input current. A first order inductive filter is considered in this dissertation for the VSI based drives. Using a higher order filter may be necessary or desirable to reduce the size and the cost [12, 77].

It is clear from (4.1) that the largest inductance is required at the lowest switching frequency for the same peak-to-peak ripple, and that the peak-to-peak ripple is linear with $1/f_{\text{sw}}$. It is reasonable to expect that the harmonic content would also be proportional to the inverse of the switching frequency.

Fig. 4.8 shows the input current harmonic content at operating points OP2–OP5 for two different cases: in one case L_f is held constant and equal to the filter inductor designed for the matrix converter drives in Table 2.10; in the other case, the product $L_f f_{\text{sw}}$ is held constant. For the latter case, L_f at $f_{\text{sw}} = 6\,\text{kHz}$ is such that the reactance $\omega_{\text{base}} L_f$ is 0.05 pu where ω_{base} is the nominal grid angular frequency.

Since L_f in Table 2.10 is 0.0261 pu, the input current harmonic content characteristics for L_f = constant and $L_f f_{\text{sw}}$ = constant meet at $f_{\text{sw}} \approx 12\,\text{kHz}$.

The harmonic content is nearly constant when $L_f f_{\text{sw}}$ is held constant; and nearly linear with $1/f_{\text{sw}}$ when L_f is held constant. This result can be used to simplify the task

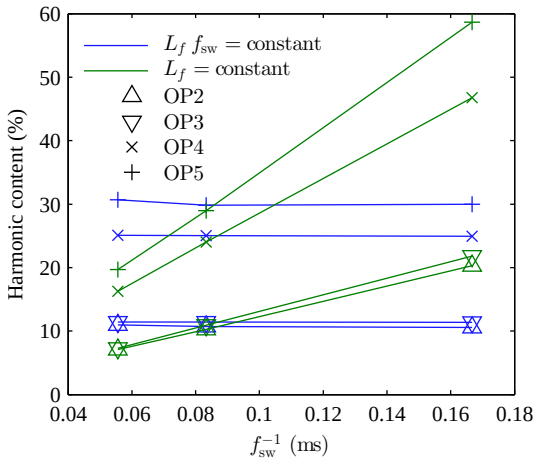


Figure 4.8: L_f and input current harmonic content for a 2L-VSI front-end.

of input inductor comparison — instead of designing filters for all three drives (2L-BBC, 3L-BBC, IMC OE Wdg.) to meet some specification and then comparing the size of the input inductor, same input inductor will be used for all three drives at all operating points, and the input current harmonic content would be compared. It is obvious that a lower harmonic content would translate into a lower input inductor requirement for meeting the same input current harmonic specification.

DC bus capacitor

It was shown in Fig. 1.2(b) that the size of the DC bus capacitor in drives applications is dictated not by the task of filtering the PWM current ripple, but by the task of absorbing the torque ripple. Let us, somewhat arbitrarily, put a limit of 5% on the peak-to-peak ripple in the DC bus voltage. For a DC bus voltage of 800 Volts, this specification restricts the DC voltage within $800 \pm 20\,\mathrm{V}$ at the torque transients with the largest amplitude $-T_{\mathrm{rated}} \leftrightarrow T_{\mathrm{rated}}$. Fig. 4.9 shows the DC bus ripple at a load torque transient $-T_{\mathrm{rated}} \rightarrow T_{\mathrm{rated}}$ for three different values of DC bus capacitance chosen such that $C_{DC} f_{\mathrm{sw}}$ is constant.

The ratio C_{DC}/I_{base} to meet the DC bus voltage specification was arrived at by simulations at $f_{\mathrm{sw}} = 12\,\mathrm{kHz}$. Starting from $C_{DC}/I_{\mathrm{base}} = 30\,\mu\mathrm{F/A}$, the ratio was reduced until the ripple voltage exceeded +2.5%.

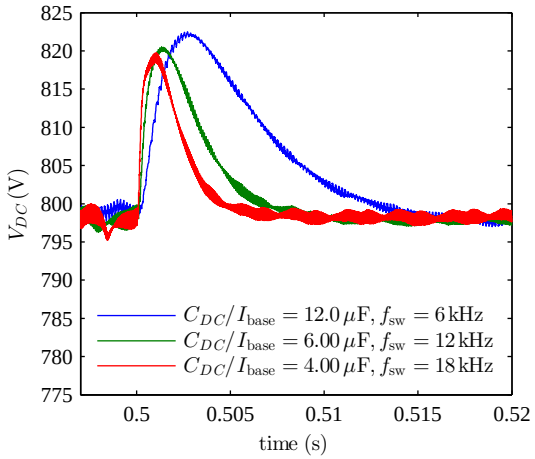


Figure 4.9: C_{DC} and DC bus voltage ripple for a 2L-BBC drive.

To understand the reduction in the value of the capacitance required with increasing switching frequency ($C_{DC} f_{\text{sw}} = \text{constant}$), the front-end controller design needs to be considered. The front-end controller has a nested control loop architecture with inner current loops and outer voltage and reactive power loops. The gain crossover frequency of the inner loops is set to be approximately a tenth of the switching frequency. Increasing the switching frequency has the effect of increasing the gain crossover frequency and thus, the closed-loop bandwidth. Consequently, the perturbations in the DC bus voltage (due to torque ripple in the load) can be corrected faster.

Fig. 4.9 also suggests that the capacitance could be reduced further with the switching frequency for the same DC bus voltage ripple ($C_{DC}^{k} f_{\text{sw}} = \text{constant}, k > 1$). However, the rule $C_{DC} f_{\text{sw}} = \text{constant}$ for determining the DC bus capacitance is deemed good enough for the purpose of this dissertation. The value of C_{DC} would be chosen from Fig. 4.9 for different switching frequencies such that the peak DC voltage ripple is $\sim 2.5\%$ for the largest load torque step.

4.3.2 Input and output current quality

The harmonic content in the input and the output currents is shown in Fig. 4.10. The harmonic content reduces with the switching frequency as expected. The input harmonic content has not been calculated for the no-load and the standstill conditions (OP1, OP6). The output harmonic content has not been calculated for the standstill condition (OP6).

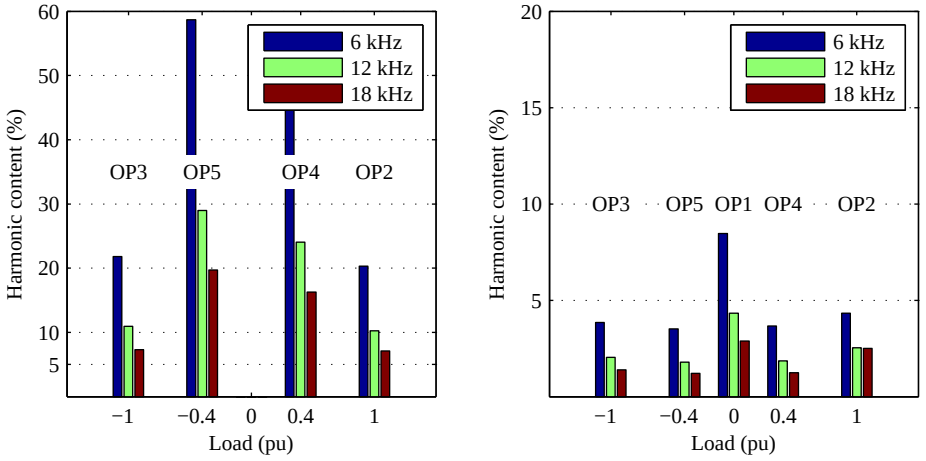
4.3.3 Semiconductor losses

The semiconductor losses in the 2L-BBC drive are shown in Fig. 4.11 for all operating points. The losses are categorized by the converter in which they occur. The semiconductor losses are shown once again in Fig. 4.12 categorized by their type (conduction v. switching).

Following observation are made:

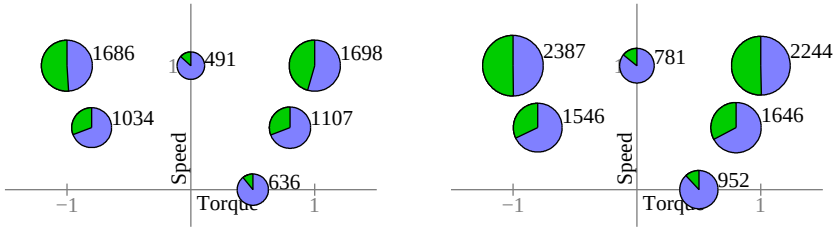
- The semiconductor losses increase with the switching frequency.
- At lower switching frequencies, the losses are dominated by the conduction losses; at higher switching frequencies, switching losses dominate.

- At lighter loads, most of the losses occur in the load-side converter (inverter).

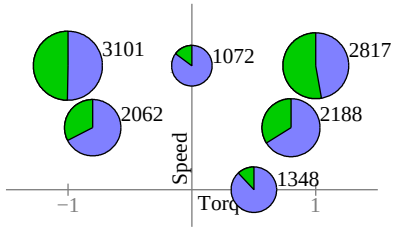


(a) Harmonic content in the input currents (b) Harmonic content in the output currents

Figure 4.10: Harmonic content in the (a) input and the (b) output currents for the 2L-BBC drive.

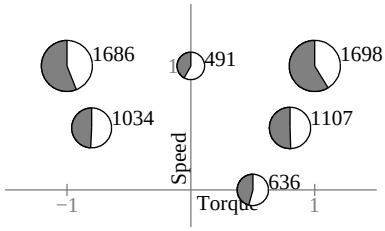


(a) Semiconductor losses at $f_{sw} = 6\,\text{kHz}$ (b) Semiconductor losses at $f_{sw} = 12\,\text{kHz}$

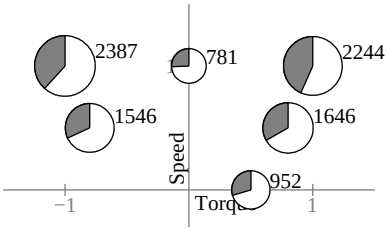


(c) Semiconductor losses at $f_{sw} = 18\,\text{kHz}$

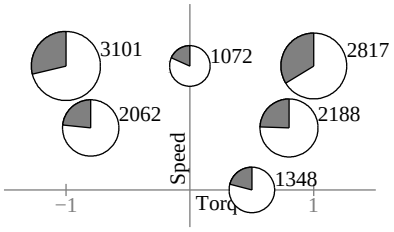
Figure 4.11: Semiconductor losses in the 2L-BBC drive. The front-end losses are represented by the green region, the inverter losses are represented by the blue region. A circle with unit diameter represents 10 kW. Rated power is 75 hp (56 kW).



(a) Semiconductor losses at $f_{\text{sw}} = 6\,\text{kHz}$



(b) Semiconductor losses at $f_{\text{sw}} = 12\,\text{kHz}$



(c) Semiconductor losses at $f_{\text{sw}} = 18\,\text{kHz}$

Figure 4.12: Semiconductor losses in the 2L-BBC drive. The conduction losses are represented by the gray region, the switching losses are represented by the white region. A circle with unit diameter represents 10 kW. Rated power is 75 hp (56 kW).

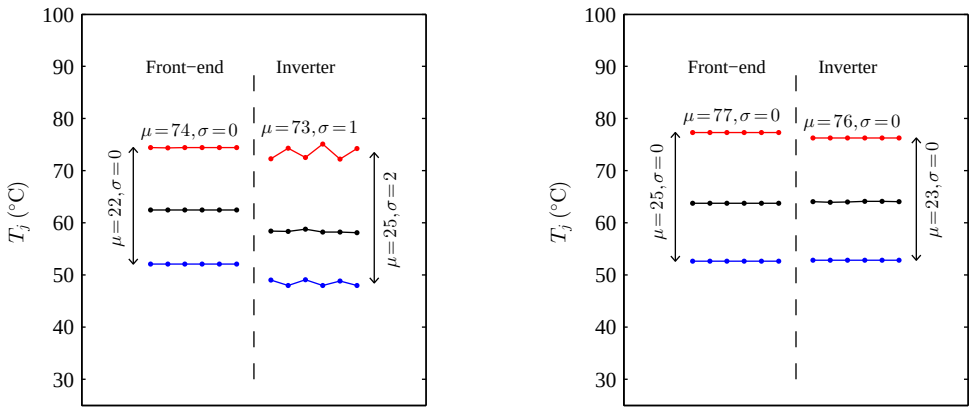
- At rated load, the front-end and the inverter incur similar losses.
- At rated load, the semiconductor losses are approximately 3%–5.5% of the rated power depending upon the switching frequency.

Distribution of the losses

In addition to the total losses in a drive, the distribution of the losses among the semiconductor devices is also an important consideration for thermal management and packaging:

- The heat sink must be designed for the semiconductor device that incurs the highest losses — symmetrical losses among all semiconductor devices are optimal for the heat sink design.
- Thermal cycling stresses the bonds at the chip and within the module leading to device failure. A semiconductor junction with minimal temperature variation is best from a reliability standpoint.

It is therefore worthwhile to analyze the distribution of the losses among the devices. Fig. 4.13 shows the junction temperatures for the operating points with the highest losses (OP2, OP3) at the highest switching frequency used.



(a) Junction temperatures at OP2, $f_{\mathrm{sw}} = 18\,\mathrm{kHz}$ (b) Junction temperatures at OP3, $f_{\mathrm{sw}} = 18\,\mathrm{kHz}$

Figure 4.13: Junction temperatures for the 2L-BBC drive.

Every dot represents a semiconductor device (the IGBT and antiparallel diode are lumped together). The blue characteristic is the minimum junction temperature reached, the red characteristic is the maximum junction temperature reached, and the black characteristic is the average junction temperature. It is desirable that the range in which the junction temperature of a given device varies be as small as possible and the maximum junction temperatures of all devices be as close as possible.

The losses in a 2L-BBC are symmetric as seen in Fig. 4.13. The 2L-BBC will be used as the reference for analyzing the symmetry of losses in other drive topologies.

4.4 Back-to-back three-level VSI (3L-BBC) based drive

This section describes the results from the simulation of the back-to-back three-level VSI (3L-BBC) drive shown in Fig. 4.6. Symmetrical SVPWM is used for all operating points (OP1–OP6) and switching frequencies ($6, 12, 18\,\mathrm{kHz}$).

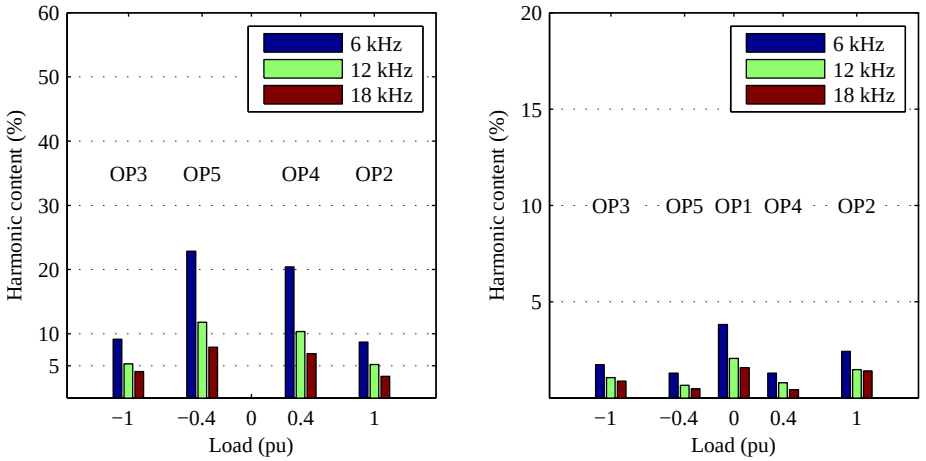
4.4.1 Passive components

The 3L-BBC drive also requires input inductors and DC bus capacitors. The discussion pertaining to the passive component sizing for the 2L-BBC drive (Section 4.3.1) can be extended to this case. Same value of the input inductance as the two-level drive (and the matrix converter based OE Wdg. drive) will be used. A higher or lower input current harmonic content would simply translate into a higher or lower input inductor requirement for meeting the same input current harmonic content specification — the conclusions will remain unaffected by the specific value of the inductance used for simulation. It is for consistency in comparison that the same value of inductance is chosen for all drive topologies.

The task of regulating the DC bus is with the front-end converter in the VSI based drives of Figs. 4.5 and 4.6. The DC bus voltage controller generates a d-axis current reference and the current controller generates a voltage reference for the front-end AC voltage based on this current reference. This part is identical in the two- and three-level back-to-back VSI drives. Since the same load and the same DC bus voltage are used for both VSI based drives, the capacitance requirements are identical to meet the DC bus ripple voltage specification. However, to attain the same effective capacitance, the individual capacitances in a 3L-BBC need to be doubled since they are series connected. Of course, they are only charged to half the DC bus voltage. Therefore, in terms of the energy stored in the DC bus ($\sum CV^2$), the two- and the three-level back-to-back drives have identical capacitance requirement. The value of the effective capacitance will be determined from Fig. 4.9: the individual capacitances used will be twice this value.

4.4.2 Input and output current quality

The harmonic content in the input and the output currents is shown in Fig. 4.14. As observed for the 2L-BBC drive, the harmonic content reduces with the switching frequency. For the same input inductance and the same load, the harmonic content in the input/output currents is lower than the two-level drive as expected. The input harmonic content has not been calculated for the no-load and the standstill conditions (OP1, OP6). The output harmonic content has not been calculated for the standstill condition (OP6).



(a) Harmonic content in the input currents (b) Harmonic content in the output currents

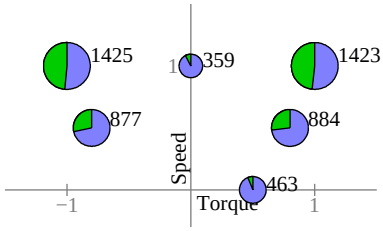
Figure 4.14: Harmonic content in the (a) input and the (b) output currents for the 3L-BBC drive.

4.4.3 Semiconductor losses

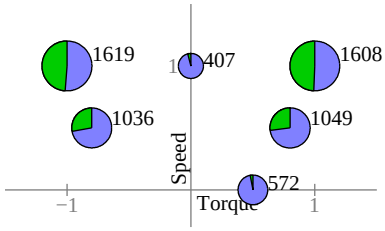
The semiconductor losses in the 3L-BBC drive are shown in Fig. 4.15 for all operating points. The losses are categorized by the converter in which they occur. The same semiconductor losses categorized by their type (conduction v. switching) are shown in Fig. 4.16.

Following are observed:

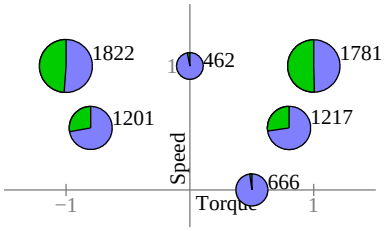
- The semiconductor losses increase with the switching frequency.
- The semiconductor losses are dominated by the conduction losses at all switching frequencies.
- At lighter loads, most of the losses occur in the load-side converter (inverter).
- At rated load, the front-end and the inverter incur similar losses.
- At rated load, the semiconductor losses are approximately 2.5%–3.25% of the rated power depending upon the switching frequency.



(a) Semiconductor losses at $f_{sw} = 6\,\text{kHz}$

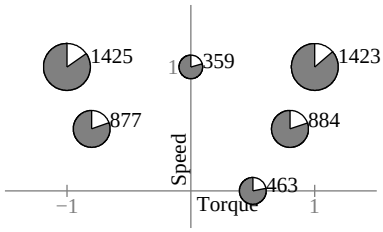


(b) Semiconductor losses at $f_{sw} = 12\,\text{kHz}$

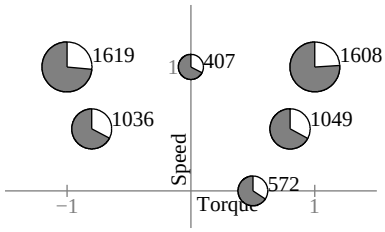


(c) Semiconductor losses at $f_{sw} = 18\,\text{kHz}$

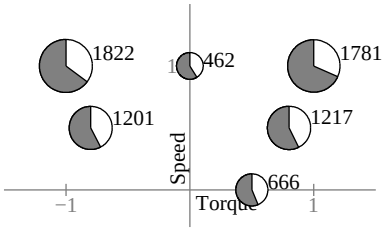
Figure 4.15: Semiconductor losses in the 3L-BBC drive. The front-end losses are represented by the green region, the inverter losses are represented by the blue region. A circle with unit diameter represents 10 kW. Rated power is 75 hp (56 kW).



(a) Semiconductor losses at $f_{sw} = 6\,\text{kHz}$



(b) Semiconductor losses at $f_{sw} = 12\,\text{kHz}$

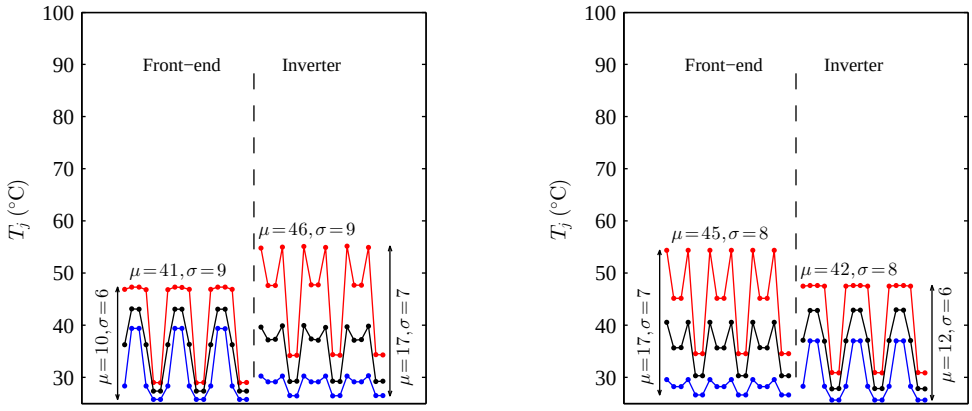


(c) Semiconductor losses at $f_{sw} = 18\,\text{kHz}$

Figure 4.16: Semiconductor losses in the 3L-BBC drive. The conduction losses are represented by the gray region, the switching losses are represented by the white region. A circle with unit diameter represents 10 kW. Rated power is 75 hp (56 kW).

Distribution of the losses

The junction temperatures for the operating points OP2 and OP3 at $f_{\mathrm{sw}} = 18\,\mathrm{kHz}$ are shown in Fig. 4.17. The range in which the temperature of a given device varies, and the maximum temperature a given device attains, are both lower than the two-level drive. However, significant variance exists in the maximum temperature attained among different devices.



(a) Junction temperatures at OP2, $f_{\mathrm{sw}} = 18\,\mathrm{kHz}$ (b) Junction temperatures at OP3, $f_{\mathrm{sw}} = 18\,\mathrm{kHz}$

Figure 4.17: Junction temperatures for the 3L-BBC drive.

4.5 T-type indirect matrix converter based open-end winding drive

The aim of this chapter is to compare the matrix converter based open-end winding drives, that are the topic of this dissertation, against the state-of-the-art drive systems. A comparison of the common-mode performance of the matrix converter drives was conducted in a previous section that showed near complete elimination of shaft voltage and therefore the detrimental bearing currents. This section will present the simulation results of the input/output waveform quality and semiconductor losses in a matrix converter based open-end winding drive for a typical industrial motor. Based on a similar analysis conducted in the last chapter comparing the matrix converter based drives against one another, the T-type indirect matrix converter based open-end winding

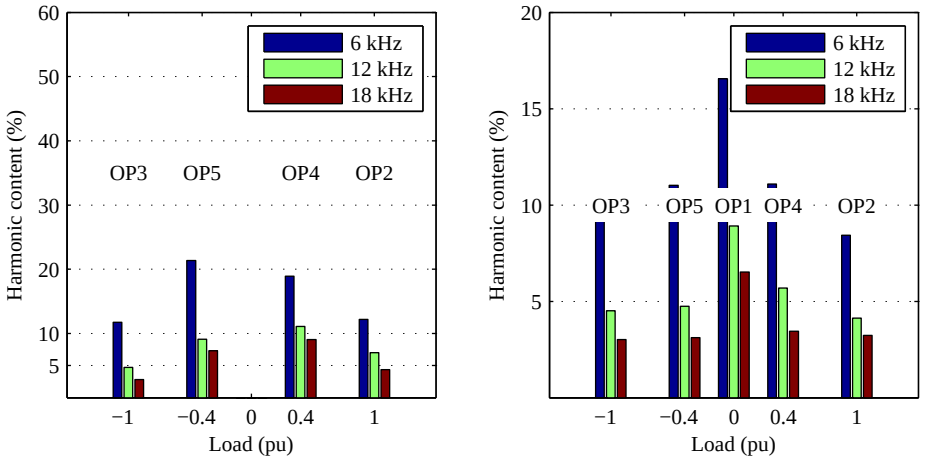
drive is chosen as the representative topology.

4.5.1 Passive components

The filter design of Table 2.10 will be used for the input current filter. The only additional passive component required is the brake resistor which is assumed to be the same for the VSI based drives as well. The inductance L_f used in this filter has been employed as the input inductor in the VSI based drives, results for which have already been presented.

4.5.2 Input and output current quality

The harmonic content in the input and the output currents is shown in Fig. 4.18. The harmonic content reduces with the switching frequency as expected. The input current harmonic content is similar or better than the VSI based drives but the output current quality is poorer. This will be discussed in more detail later. The input harmonic content has not been calculated for the no-load and standstill conditions (OP1, OP6). The output harmonic content has not been calculated for the standstill condition (OP6).



(a) Harmonic content in the input currents (b) Harmonic content in the output currents

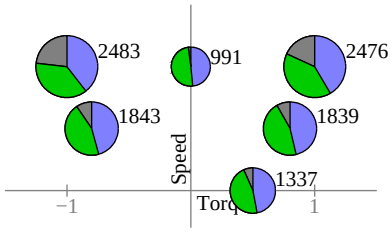
Figure 4.18: Harmonic content in the (a) input and the (b) output currents for the T-type IMC OE Wdg. drive.

4.5.3 Semiconductor losses

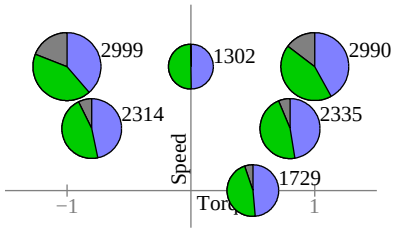
The semiconductor losses in the T-type IMC OE Wdg. drive are shown in Fig. 4.19 for all operating points. The losses are categorized by the converter in which they occur. The same semiconductor losses categorized by their type (conduction v. switching) are shown in Fig. 4.20.

Following are observed:

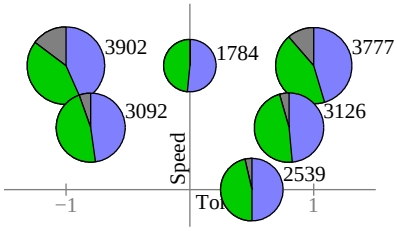
- The semiconductor losses increase with the switching frequency.
- The semiconductor losses are dominated by the switching losses at $f_{\text{sw}} = 18\,\text{kHz}$, and by the conduction losses at lower switching frequencies.
- Most of the losses occur in the load-side PWM converters; the front-end converter only incurs conduction losses.
- At rated load, the semiconductor losses are approximately 4.5%–7% of the rated power depending upon the switching frequency.



(a) Semiconductor losses at $f_{\text{sw}} = 6\,\text{kHz}$

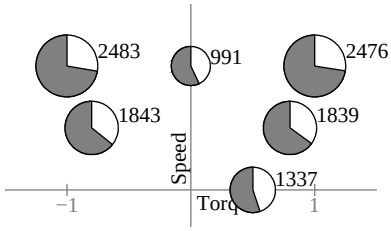


(b) Semiconductor losses at $f_{\text{sw}} = 12\,\text{kHz}$

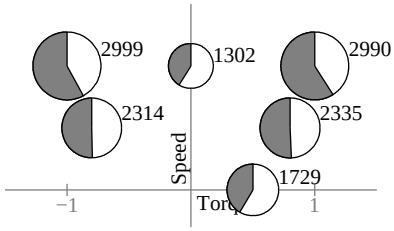


(c) Semiconductor losses at $f_{\text{sw}} = 18\,\text{kHz}$

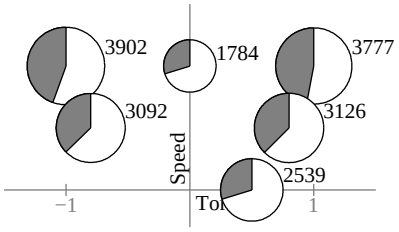
Figure 4.19: Semiconductor losses in the T-type indirect matrix converter based open-end winding drive. The front-end losses are represented by the gray region; the blue and the green region represent the losses in the load-side PWM converters. A circle with unit diameter represents 10 kW. Rated power is 75 hp (56 kW).



(a) Semiconductor losses at $f_{\text{sw}} = 6\,\text{kHz}$



(b) Semiconductor losses at $f_{\text{sw}} = 12\,\text{kHz}$



(c) Semiconductor losses at $f_{\text{sw}} = 18\,\text{kHz}$

Figure 4.20: Semiconductor losses in the T-type indirect matrix converter based open-end winding drive. The conduction losses are represented by the gray region, the switching losses are represented by the white region. A circle with unit diameter represents 10 kW. Rated power is 75 hp (56 kW).

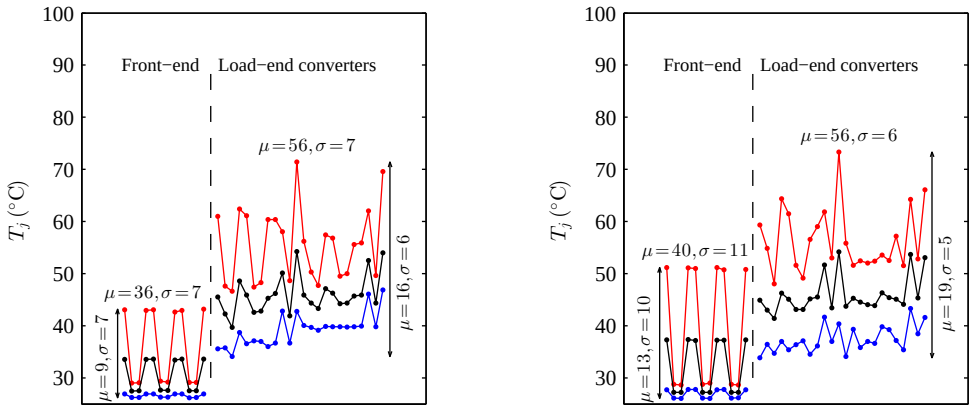
Distribution of the losses

The junction temperatures for the operating points OP2 and OP3 at $f_{\text{sw}} = 18\,\text{kHz}$ are shown in Fig. 4.21. The front-end converter of this drive has lower losses and lower junction temperatures compared to the front-end converters in the VSI based drives. Further discussion the distribution of losses is reserved for next section.

4.6 Comparison and conclusions

The passive component requirements, input/output waveform quality with the same input inductor, semiconductor losses and the distribution of semiconductor losses among devices were analyzed in this chapter for the two- and three-level back-to-back VSI drives and the T-type IMC OE Wdg. drive using simulations of a typical industrial motor drive at several operating points. The common-mode output characteristic of the three drives were compared using experimental results at low voltage and power.

This section uses compares the results from the previous sections to determine if the



(a) Junction temperatures at OP2, $f_{\text{sw}} = 18\,\text{kHz}$ (b) Junction temperatures at OP3, $f_{\text{sw}} = 18\,\text{kHz}$

Figure 4.21: Junction temperatures for the T-type IMC OE Wdg. drive.

T-type IMC OE Wdg. drive has the potential to replace the VSI based drives as the state-of-the-art.

4.6.1 Passive components and input current quality

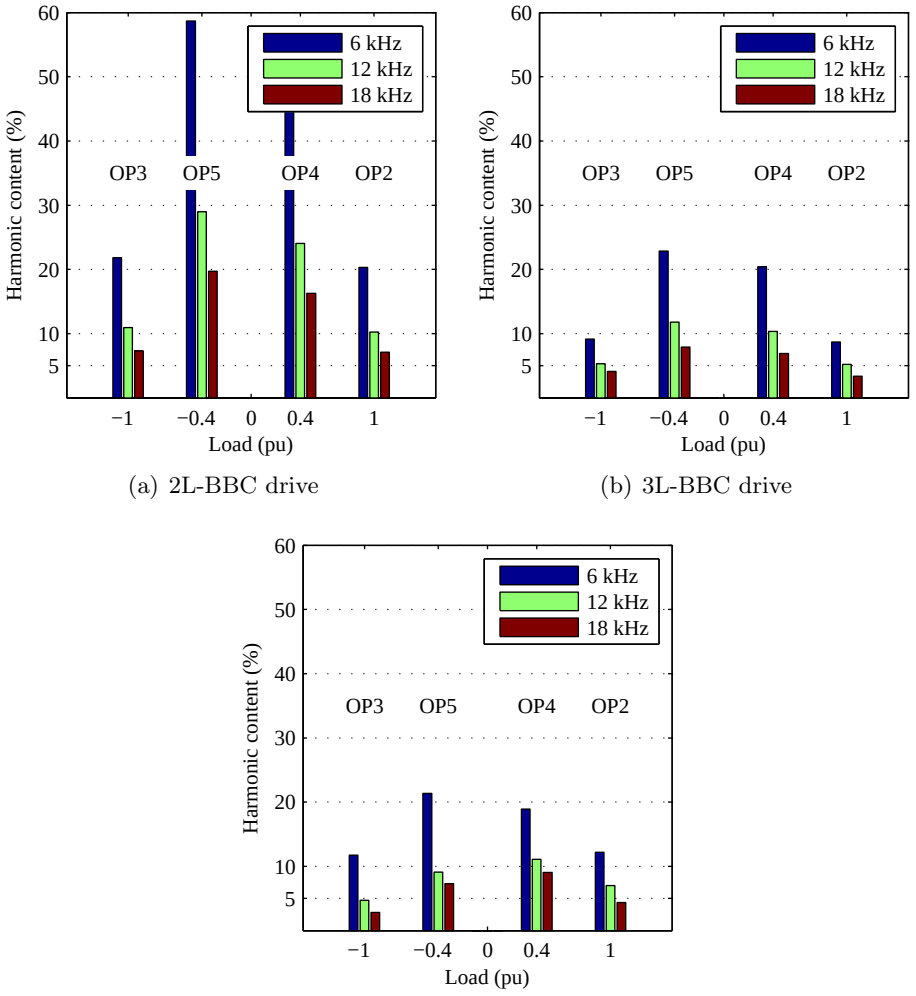
The harmonic content in the input currents for the three drives has been reproduced in Fig. 4.22. All three drives use the same input inductance (L_f from Table 2.10). The harmonic content falls as the switching frequency is increased. A three-level VSI front-end offers better harmonic performance than a two-level as expected.

Inductance

The inductance used is the main filter inductance of the third-order filter designed for the matrix converter based open-end winding drives in Chapter 2. The harmonic content in the T-type IMC OE Wdg. drive is greater than 10% at $f_{\text{sw}} = 6\,\text{kHz}$. This is not unexpected because the filter design was based on the unfiltered input current spectra at $f_{\text{sw}} = 12\,\text{kHz}$. Considering only the data at $f_{\text{sw}} = 12\,\text{kHz}$ and 18 kHz, it is seen from Fig. 4.22 that the input current harmonic content in the T-type drive is similar to that in the 3L-VSI front-end, e.g. the harmonic content is lower with the 3L-VSI front-end at OP2 whereas it is lower with the T-type drive at OP3 etc. Therefore it could be concluded that the filter inductance requirements of the T-type drive are similar to the

3L-BBC drive. The contribution of the damping inductor L_d used in the T-type drive's input filter to the total magnetics requirements is small due to its significantly smaller size.

It was shown in Section 4.3.1 that the linear dependence of the peak-to-peak input current ripple on the $L_f f_{\text{sw}}$ product also translates into an approximately linear dependence of the input current harmonic content on this product. Therefore, to achieve a



(a) 2L-BBC drive

(b) 3L-BBC drive

(c) T-type IMC OE Wdg. drive

Figure 4.22: Input current harmonic content for the (a) 2L-BBC, (b) 3L-BBC, and (c) T-type IMC OE Wdg. drives.

similar harmonic content as the three-level and T-type IMC OE Wdg. drive, an input inductor approximately twice its current value would need to be used in the 2L-BBC drive.

In summary, the inductor requirements in the back-to-back VSI drives when using a purely inductive first-order filter are similar to the T-type IMC OE Wdg. drive for a three-level drive, and approximately twice as much for a two-level drive.

Capacitance

The analysis in the last section for the T-type IMC OE Wdg. drive used a filter design based on the input current spectrum at $f_{\text{sw}} = 12\,\text{kHz}$. The damped resonant frequency ω_d of this filter is such that $10\,\omega_d < \omega_{\text{sw}}$ where $\omega_{\text{sw}} = 2\pi f_{\text{sw}}$. Same attenuation as $f_{\text{sw}} = 12\,\text{kHz}$ can be achieved at a switching frequency $f_{\text{sw}} = 18\,\text{kHz}$ at a higher ω_d, i.e. the capacitance and the inductance can be reduced by a factor of $3/2$ at $f_{\text{sw}} = 18\,\text{kHz}$ while maintaining the attenuation at f_{sw} and its multiples. The capacitance requirements of the T-type IMC OE Wdg. drive (and the other matrix converter based open-end winding drives) are therefore inversely proportional to the switching frequency.

The DC bus capacitance for the VSI based drives is selected based on Fig. 4.9. The capacitance used to meet the DC bus voltage ripple specification is once again inversely proportional to the switching frequency. Therefore, the comparison of the capacitance requirements of the drives can be conducted at $f_{\text{sw}} = 12\,\text{kHz}$ with the understanding that the capacitance required falls inversely with the switching frequency for all of the drives considered.

Component values

The approximate inductance required by the three drives to achieve an input current harmonic content $\sim 5\%$ at $f_{\text{sw}} = 12\,\text{kHz}$ ($200 f_{\text{grid}}$) and the rated load (motoring or generating) are shown in Table 4.5. The values of the capacitance required to maintain the DC bus voltage within 5% of its nominal value in the voltage link drives, and the filter capacitance required in T-type IMC OE Wdg. drive are also shown in this table. All inductors, with the exception of the damping inductance L_d, need to be rated for the same current. The inductor L_d has approximately a third the inductance of L_f and is required to carry approximately a tenth the current. Assuming the product LI^2 to

be an indicator of the size and the cost, it is seen that the contribution of L_d toward the total magnetics requirements is insignificant.

The DC bus capacitance for the 3L-BBC drive is the *effective* capacitance — two capacitors twice the capacitance and half the voltage rating would be connected in series to form the DC bus. Assuming the product CV^2 to be an indicator of the size and the cost, it is seen that the DC bus capacitance requirements of the two-level and three-level back-to-back VSI based drives are identical.

Three capacitors are required in the T-type IMC OE Wdg. drive. The capacitance in Table 4.5 is in per-unit — either three capacitors corresponding to the absolute value of 0.1631 pu could be connected in a wye-configuration, or three capacitors with third the capacitance but $\sqrt{3}$ times the voltage rating could be connected in a delta configuration as shown in Fig. 1.9(b). In both the configurations, the CV^2 product is $C_f C_{\text{base}} V_{\text{base}}^2$, where C_f is expressed in per-unit and is equal to 0.1631 pu (for the filter of Table 2.10).

The actual voltage that appears across the three delta connected capacitors in the soft link of the indirect matrix converter drive is not the line-to-line voltage — it is a rectified voltage with a smaller AC component. The low-frequency current in the capacitors connected across $v_{\text{max}}, v_{\text{mid}}$ and across $v_{\text{mid}}, v_{\text{min}}$ is higher than the current in the capacitor connected across $v_{\text{max}}, v_{\text{min}}$. However, the film capacitors that would be used in such an application are rated for much larger ripple currents and the slight asymmetry is not an issue.

Overall, the T-type IMC OE Wdg. drive, therefore all matrix converter based open-end winding drives, requires significantly lower capacitance compared to the voltage link

	Two-level back-to-back	Three-level back-to-back	T-type IMC OE Wdg.
Inductance	5%–6%	2.5%–3%	2.5%–3% (2.61%)
Capacitance	63%	63%	16% (16.31%)
Damping branch inductor, L_d	N/A	N/A	0.75%–1%(0.83%)
Damping resistor, r_d	N/A	N/A	$\sim$ 55% (55.47%)

Table 4.5: A comparison of the passive element requirements of the T-type IMC OE Wdg. drive against the back-to-back VSI drives. Values in the parenthesis correspond to Table 2.10. All values are per-unitized for a 480 V, 80 kVA system.

drives. The inductance required to achieve similar input current quality is similar to the 3L-BBC drive, and approximately half of the inductance required in the 2L-BBC drive.

4.6.2 Output current quality

The harmonic content in the output currents for the three drives has been reproduced in Fig. 4.23. Across all switching frequencies and operating points, the 3L-VSI has the lowest harmonic content in the output current, followed by the 2L-VSI. The harmonic content is highest in the matrix converter based drive.

Weighted total harmonic distortion (WTHD) is often used as a measure of the harmonic performance of a given drive topology and modulation strategy [2],

$$\text{WTHD} = \sqrt{\sum_{n=2}^{\infty} \left(\frac{V_n}{n V_1} \right)^2} \tag{4.2}$$

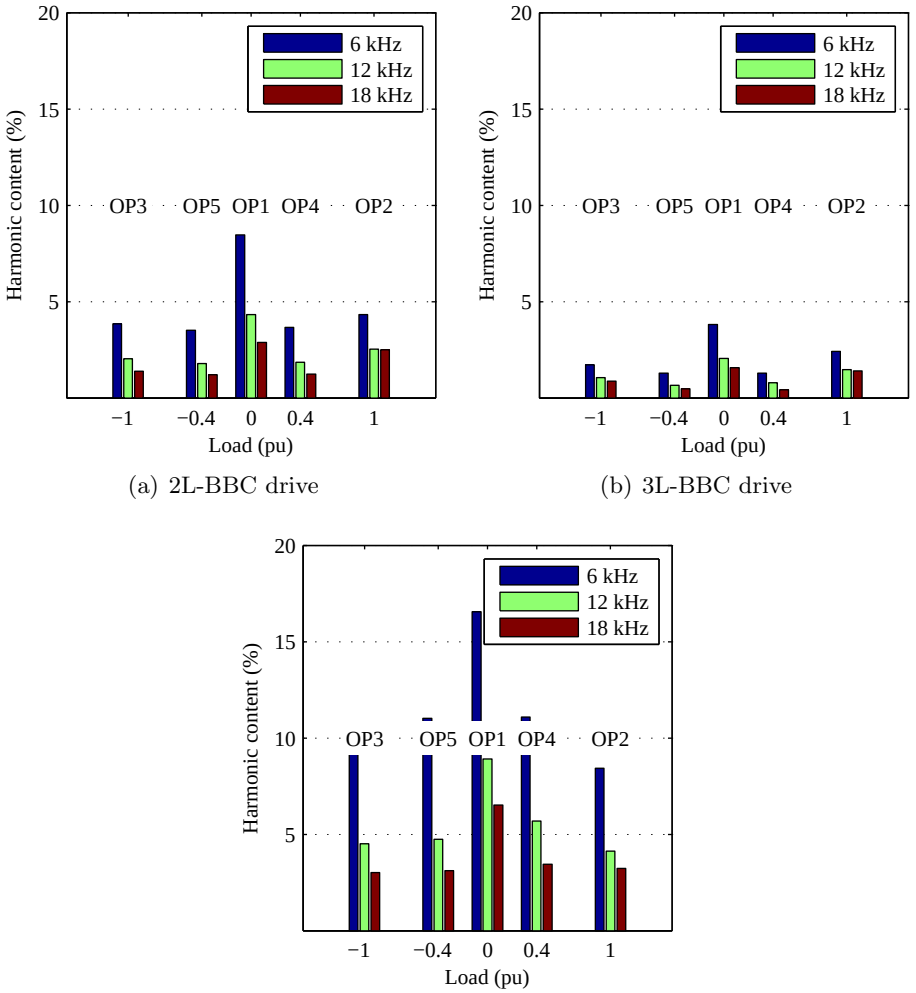
where n is the harmonic order. The WTHD for the drives being compared is shown in Table 4.6 at some operating conditions. The load voltage being generated is proportional to the output fundamental frequency f_{out} (V/f). For $f_{\text{out}} = 60\,\text{Hz}$, output voltage is equal to V_{base}. The results in Table 4.6 and in Fig. 4.23 show that the matrix converter based open-end winding drives have a higher harmonic content in the generated output.

The superiority of the three-level inverter is also supported by the experimental results (from low power prototypes) shown in Fig. 4.24. However, the amplitude of the components at the switching frequency and its multiples is similar for the two-level and the matrix converter based open-end winding drives even though Fig. 4.23 and Table 4.6 suggest that the high-frequency components would be lower in the two-level drive.

The explanation for this anomaly lies in the output voltage harmonic content against the voltage transfer ratio characteristics of the matrix converter based open-end winding drives discussed in Chapter 3 — the output voltage harmonic content in the MC OE

	Three-level	Two-level	T-type IMC OE
30 Hz	0.16%	0.34%	0.86%
60 Hz	0.17%	0.41%	1.00%

Table 4.6: WTHD for different drives at $f_{\text{out}} = 30\,\text{Hz}$ and $60\,\text{Hz}$ and $f_{\text{sw}} = 6\,\text{kHz}$.



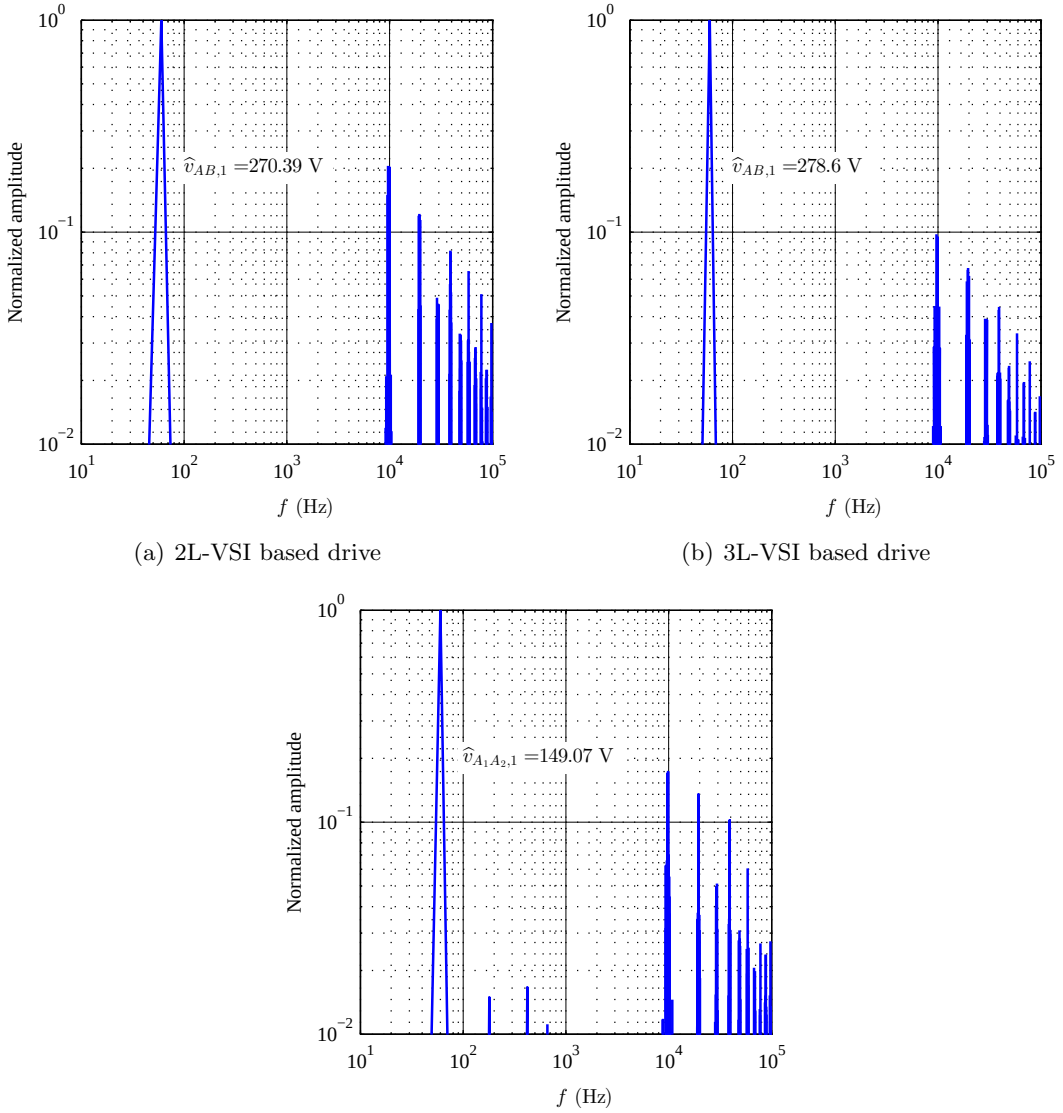
(a) 2L-BBC drive

(b) 3L-BBC drive

(c) T-type IMC OE Wdg. drive

Figure 4.23: Output current harmonic content for (a) 2L-BBC, (b) 3L-BBC, and (c) T-type IMC OE Wdg. drives.

Wdg. drives declines with the voltage transfer ratio. The IMC OE Wdg. drive is operating close to the full voltage transfer ratio of 1.50 in Fig. 4.24(c) leading to a lower output voltage harmonic content. In contrast, the voltage transfer ratio for the results in Fig. 4.23(c) is unity or lower — if the input voltage were to be stepped down, and the IMC OE Wdg. drive was then operated at a higher voltage transfer ratio, the output voltage harmonic content would decline.



(a) 2L-VSI based drive

(b) 3L-VSI based drive

(c) IMC OE Wdg. drive

Figure 4.24: Experimental spectra of the output voltage for (a) 2L-VSI, (b) 3L-VSI, and (c) I-type IMC OE Wdg. drives. $f_{\text{out}} = 60\,\text{Hz}$, $V_{\text{out}} = 200\,\text{V}$.

4.6.3 Semiconductor losses and their distribution

The semiconductor loss results from previous sections have been reproduced in Fig. 4.25. The T-type IMC OE Wdg. drive was shown to have minimum losses among the matrix

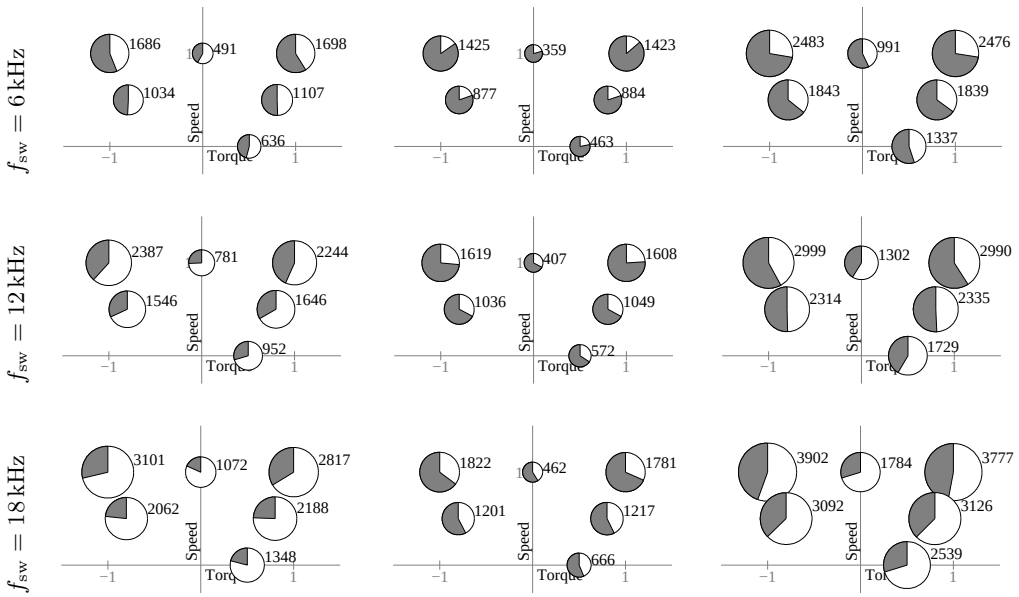


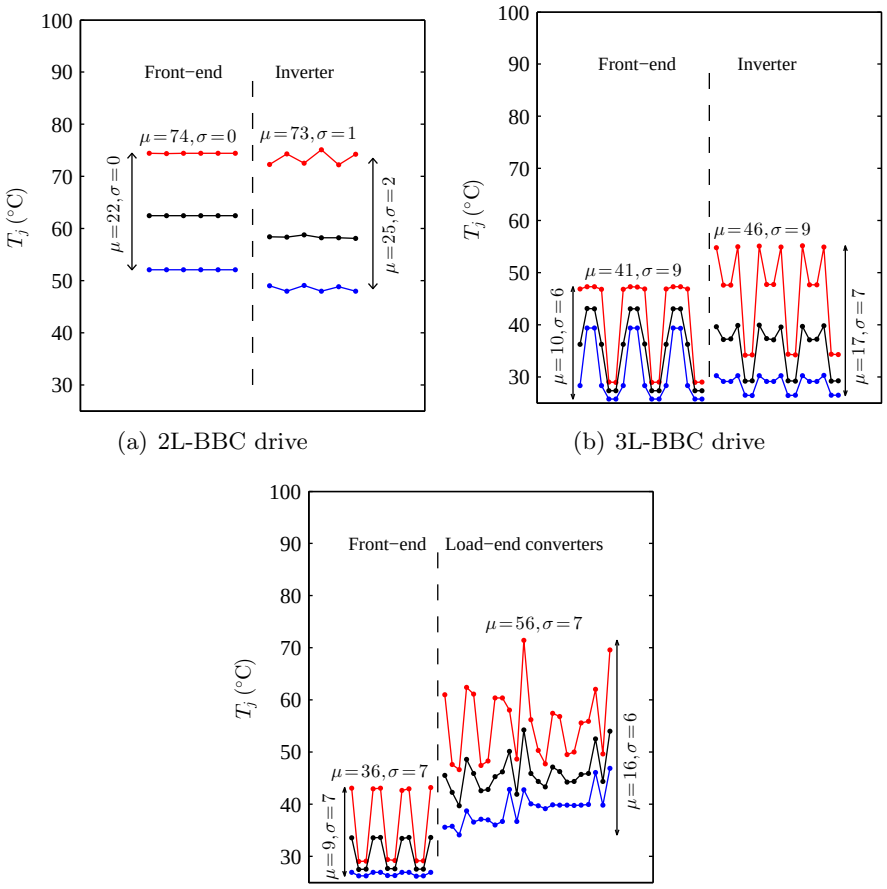
Figure 4.25: Semiconductor losses in the three drives. The gray regions represent the conduction losses. A circle with unit diameter represents 10kW. Rated power is 75hp (56kW).

converter based open-end winding drives in the previous chapter. Yet this drive has the highest losses when compared to the state-of-the-art drives, followed by the 2L-BBC drive. The 3L-BBC drive has the minimum losses.

Even though the number of devices conducting and switching in the 3L-BBC drive is higher than the 2L-BBC drive, the losses are lower because of the device used — the conduction losses and the diode reverse recovery losses are significantly lower in the 600 V device as compared to the 1200 V device. The T-type IMC OE Wdg. drive and the 2L-BBC drive use the same 1200 V IGBT/diode. The conduction losses in the T-type drive are, of course, higher due to a higher number of devices active at any given time.

The plots showing the estimated junction temperatures (and thus the distribution of losses among the devices) for OP2 (synchronous speed, rated torque) are reproduced in Fig. 4.26.

The highest temperatures are reached in the two-level drive due to the losses being



(a) 2L-BBC drive

(b) 3L-BBC drive

(c) T-type IMC OE Wdg. drive

Figure 4.26: Distribution of losses among semiconductor devices at OP2, $f_{\text{sw}} = 18\,\text{kHz}$.

distributed among fewer devices. The losses are most symmetric in this drive. Even though the mean value of the junction temperature variation is higher in the 2L-BBC drive, the maximum value of the junction temperature variation is higher in the other two drives. The T-type IMC OE Wdg. drive and the 3L-BBC drive have similar variation in the junction temperatures. A clear pattern in the T-type drive is not seen (as compared to the other two) because the distribution of the losses among the devices keeps changing slowly enough to overcome the time constant of the thermal circuit. Therefore considerably longer simulations are required to reveal the distribution — however, it was verified that the reported results capture the maximum junction

temperatures reached. Since the maximum junction temperatures in the 3L-BBC drive also exhibit a high variance, the heat sink design procedures for three-level inverters could be adapted for the T-type IMC OE Wdg. drives. Of course, the heat sink would need to be sized to accommodate the higher losses.

In the simulations, an isothermal heat sink with infinite heat capacity was assumed. The estimated junction temperatures with this heat sink are considerably lower than the absolute maximum specifications for all three drives. Therefore it is expected that the drives should be able to function without the risk of immediate failure even with a real heat sink. The junction temperature and the losses shown are for steady state conditions. Significantly higher losses and junction temperatures were observed during transients — no attempt was made to slow the transients down in the interest of the simulation time. In a practical drive, imposing limits on the device currents will have the effect of limiting the losses during transients and keeping the junction temperatures within the specifications.

4.6.4 Semiconductor requirements, instrumentation, and control

The devices used in the simulations were selected such that the steady state voltages and currents were limited to two-thirds of the absolute maximum ratings. The T-type drive used a total of 36 IGBTs with antiparallel diodes rated for 1200 Volts and 200 Amperes. Let the semiconductor requirements be quantified by the cumulative product of the voltage and the current ratings of the devices used:

$$\begin{aligned} \mathcal{V}_{\text{T-type}} &= 36 \times 2 \times 1200 \times 200 \\ &= 17.28\,\text{MVA} \end{aligned} \tag{4.3}$$

$\mathcal{V}$ can similarly be defined for the voltage link drives to compare the semiconductor requirements.

The voltage link drives (2L-BBC, 3L-BBC) use a decoupled control architecture — the input and the output currents are controlled independent of each other. A front-end controller and input current feedback are required in addition to the motor controller to control the input currents. In contrast, in a matrix converter based drive, generating sinusoidal load voltages ensures that the input currents are sinusoidal as well, as long

as the load is balanced. The instrumentation and control requirements of the matrix converter drives are therefore lower than the voltage link drives.

4.6.5 Comparison and conclusions

With the requirements and the characteristics of the drives established, they are compared qualitatively and quantitatively in Table 4.7. The high-frequency common-mode performance of the I-type IMC OE Wdg. drive, and by extension all matrix converter based open-end winding drives discussed in this dissertation, is better than the VSI based state-of-the-art drives. The capacitance requirements of the matrix converter based open-end winding drives are also lower than the state-of-the-art. Thus, matrix converter based OE Wdg. drives solve the major drawbacks of the industry standard VSI based drives. Lower instrumentation and control requirements are the further advantages of the matrix converter approach.

However, as seen from Table 4.7, the higher semiconductor requirements, higher

		Two-level	Three-level	T-type
Common-mode	Shaft voltage	High	Medium	Near-zero
	Ground currents	High	Medium	Low
	LF CM current	–	–	High
Semiconductor losses	% of the rated output	3%–5.5%	2.5%–3.25%	4.5%–7%
Semiconductor requirements	Cumulative V, I product, $\mathcal{V}$	5.76 MVA	7.2 MVA	17.28 MVA
Passive elements	Input inductor	$\sim 2L_f$	L_f	L_f
	Filter/DC capacitor	$\sim 4C_f$	$\sim 4C_f$	C_f
	Damping inductor	N/A	N/A	Small
	Damping resistor	N/A	N/A	Small
Output current	WTHD at rated output ($f_{sw} = 6$ kHz)	0.41%	0.17%	1.00%
Instrumentation	AC voltage sensors	2 (3)	2 (3)	2 (3)
	AC current sensors	4 (6)	4 (6)	2 (3)
	DC voltage sensors	1	2	1
Control	Motor controller	Required	Required	Required
	Front-end controller	Required	Required	N/A

Table 4.7: Comparison of the T-type IMC OE Wdg. drive against state-of-the-art.

semiconductor losses, rather large circulating currents, and relatively poorer output voltage/current quality of the matrix converter based open-end winding drives preclude a clear choice, especially against the back-to-back three-level VSI (3L-BBC) drive.

Some of the aforementioned drawbacks of the matrix converter based open-end winding drives can be addressed by employing new semiconductor devices and by closed-loop control as discussed in the next chapter.

Chapter 5

Conclusions and further research

Detrimental common-mode voltage and a large DC bus capacitor are the major drawbacks of the state-of-the-art drive systems. Two distinct indirect matrix converter based open-end winding drive topologies that address the aforementioned problems were presented in this dissertation. Experimental results verified the theory of operation as well as the advantages of the indirect approach over the direct approach.

An optimized third-order filter design that is applicable to all matrix converter based drive systems was discussed. The size of the reactive components of the resulting filter designed using this approach was experimentally shown to be smaller than a conventional second-order filter.

Loss-optimal carrier and switching sequences were identified for the direct and the indirect matrix converter based open-end winding drives. A comparison of all matrix converter topologies based on semiconductor requirements and losses, passive element requirements, input and output waveform quality, and other features identified the T-type drive as the best matrix converter based open-end winding drive topology.

This drive was compared to the state-of-the-art drives (2L-BBC and 3L-BBC) on common-mode performance, passive element requirements, semiconductor requirements and losses, input and output waveform quality, and control and instrumentation requirements. The matrix converter based open-end winding drives were found to significantly reduce the effects of the high-frequency common-mode voltage, and significantly shrink the capacitance required. However, the VSI based state-of-the-art drives offered better output current quality and lower semiconductor losses. The matrix converter based

open-end winding drives were also found to suffer from appreciable circulating currents.

The output quality and the semiconductor losses in the matrix converter based open-end winding drives can be addressed by employing the wide band gap (WBG) devices that have become commercially available in the recent years — the switching frequency can be increased by an order of magnitude ($\sim 100\,\text{kHz}$ as opposed to $\sim 10\,\text{kHz}$) such that the high-frequency content in the output current is negligible. Wide band gap devices can also keep the semiconductor losses in check to the extent that the thermal management does not contribute to the system costs significantly.

In addition, direct torque control may be used to limit the losses at lighter loads. The circulating currents can be addressed by a zero-sequence controller, or by using dead-time compensation. By reducing the semiconductor losses and improving the output quality, including the elimination of circulating currents, indirect matrix converter drives can be made preferable to the state-of-the-art.

Natural low-voltage-ride-through (LVRT) integration was briefly discussed as an advantage of the indirect approach. Implementation of an LVRT scheme is also necessary to make the IMC OE Wdg. drives viable.

In conclusion, matrix converter based open-end winding drives succeed in reducing the effects of the output common-mode voltage and the size of the capacitor compared to the VSI based drives. Future research should include LVRT implementation, redesign of the T-type drive with WBG devices, and advanced closed-loop control of the output currents such that indirect matrix converter based open-end winding drive present a stronger case to replace the VSI based drives as the state-of-the-art.

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Appendix A

A.1 Abbreviations, acronyms, and definitions

2L-BBC	Two-level back-to-back converter
2L-VSI	Two-level voltage source inverter
3L-BBC	Three-level back-to-back converter
3L-VSI	Three-level voltage source inverter
AC	Alternating current
ACIM	AC induction machine
CMC	Conventional matrix converter
CDMC	Conventional direct matrix converter
CIMC	Conventional indirect matrix converter
CMV	Common-mode voltage
CSR	Current source rectifier
DC	Direct current
DMC	Direct matrix converter
ESL	Equivalent series inductance
ESR	Equivalent series resistance
Front-end	The input (grid) side converter in 2L-BBC, 3L-BBC, and indirect matrix converter drive topologies. Load-end converter is similarly defined.
IGBT	Insulated gate bipolar transistor
IMC	Indirect matrix converter

I-type drive	I-type indirect matrix converter based open-end winding drive
I-type IMC OE Wdg. drive	See I-type drive
MC	Matrix converter
NPC	Neutral-point-clamped three-level inverter
OE Wdg.	Open-end winding
PWM	Pulse width modulation
rms	Root mean square
SVPWM	Space vector pulse width modulation
T-type drive	T-type indirect matrix converter based open-end winding drive
T-type IMC OE Wdg. drive	See T-type drive
VFD	Variable frequency drive
VSI	Voltage source inverter

A.2 Notation

μ	Mean
σ	Standard deviation
x	A time-varying quantity
x_a	A quantity corresponding to the input (lower case subscript)
x_A	A quantity corresponding to the output (upper case subscript)
x^*	A reference/desired value
$\overline{x}$	Switching cycle average of a time-varying quantity
$\widehat{x}$	Amplitude of a time-varying quantity
X	Root mean square value of a time-varying quantity
$\vec{x}$	A space vector in the complex plane
$\mathbf{x}$	A row or a column vector
$\mathbf{X}$	A matrix
(x_1, x_2, x_3)	An ordered triplet
$\{x_1, x_2, x_3\}$	A set
$\mathbb{C}$	The set of complex numbers
$\mathbb{R}$	The set of real numbers
$\| \|_\infty$	Infinity-norm